A MULTIPLE MOTOR CONTROL SYSTEM FOR ULTRASONIC COMPUTED AXIAL TOMOGRAPHY

BY

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THESIS

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Chapter 1

Introduction

Computed Axial Tomography (CAT) has revolutionized the field of diagnostic medical imaging. The conventional CAT scanners used for diagnostic purposes in hospitals today employ X-rays as a source of radiation. A CAT scan consists of a collection of multiple attenuation measurements taken through a sample at different angles. These attenuation measurements are then used by a reconstruction algorithm to produce a cross sectional image of the "slice" of tissue through which the measurements have been taken. Through various image processing techniques, the radiographic density of the tissue within the cross-sectional image may be accurately determined.

There are two primary types of scans that may be used for gathering tomographic data: the translate-and-rotate scan and the fan-beam scan. Translate-and-rotate involves translating the radiation source and detector linearly across the specimen and rotating the source/detector reference frame at the end of each linear pass. The fan-beam scan merely rotates the source and detector array through an angle of 180 degrees. Translate-and-rotate was the earliest scan configuration and was used by EMI Medical in the original

original brain scanner (Scudder, 1978). This method has fallen out of vogue primarily because of the large amount of time taken (about 1 minute) in completing a scan. In an effort to minimize scan time, and hence radiation dosage to the patient, the fan-beam scan evolved.

Because of the difference in characteristics between X-ray radiation and ultrasonic radiation, it was believed that more information about tissue characteristics would be acquired if ultrasound were employed as a radiation source. The Bioacoustics Research Laboratory at the University of Illinois at Urbana-Champaign has embarked on the task of designing an Ultrasonic Computed Axial Tomographic (UCAT) scanner. While X-ray detectors may easily be constructed in an array configuration for parallel acquisition of fan-beam attenuation data, ultrasonic detector arrays are much more difficult to fabricate. In an effort to minimize the complexity of the detector as well as the data acquisition hardware, a hybrid "fan-sweep-and-rotate" geometry was chosen. In this configuration, the ultrasonic transmitter and receiver sweep past the specimen. As the fan motion is occurring, individual point readings are made by the Data Acquisition System (DAS) developed by Chan (1979). At the end of the fan-beam sweep, both the transmitter and receiver rotate around the specimen by an angular increment. The fan-beam motion resumes and another set of data points are taken at the new angular orientation. This scanning action

continues until the receiver and transmitter have rotated 180 degrees about the specimen.

The DAS measures the frequency dependent amplitude and time-of-flight of the ultrasonic pulse as it passes from the transmitter through the specimen to the receiver. The many parameters of the ultrasound being sent and the measurements being taken may be varied by way of computer control of the DAS.

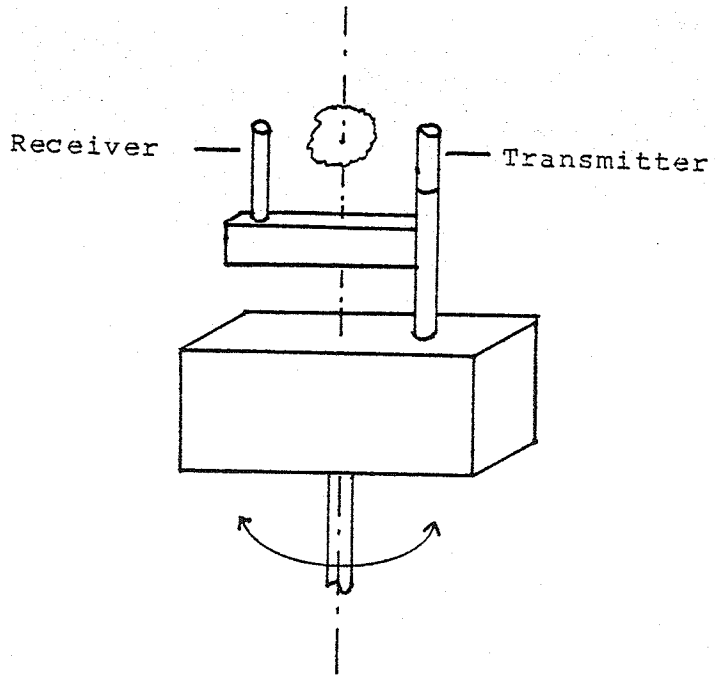
Both the fan-beam scanning motion and the rotational motion of the transmitter-receiver must be controlled in some manner. These motions constitute two degrees of freedom. A third degree of freedom allows the receiver to be offset by an angle (cocked) with respect to the transmitter. The motion of this degree of freedom must also be controlled. An Interdata Model 7/32 computer oversees the data acquisition task and directs the various degrees of freedom through their appropriate motions by way of an intelligent motor controller. This thesis describes the design of the hardware necessary to implement the microprocessor control of position and velocity of all of the degrees of freedom.

Chapter 2

System Overview

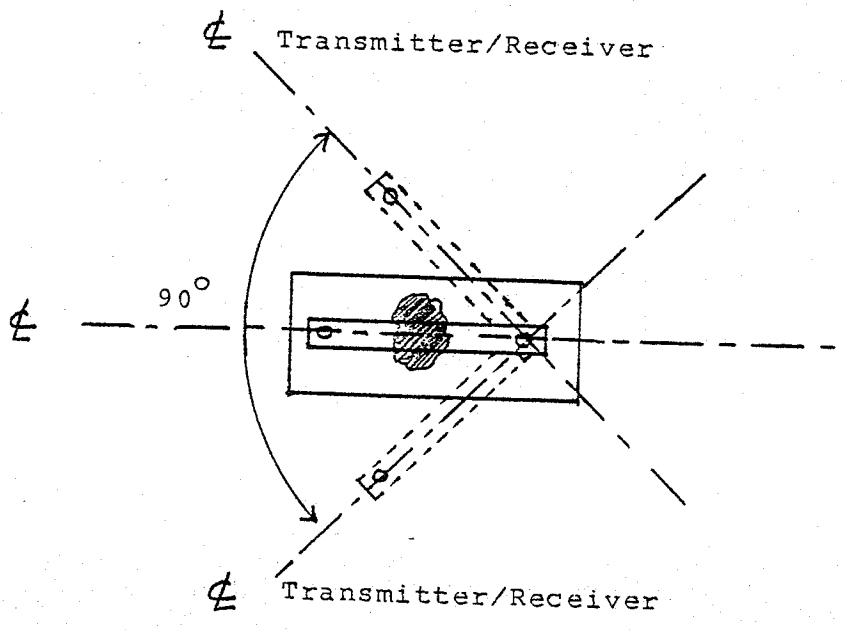
2.1 Mechanical Design of The Scanner

The initial UCAT scanner designed at The Mayo Clinic had close to the mechanical configuration of the scanner at the Bioacoustics Research Laboratory. The Mayo scanner employed a fan-sweep-and-rotate geometry having two degrees of freedom. In an effort to gather data on the refraction properties of tissue a third degree of freedom, the cocking angle was added. This degree of freedom, described in Chapter 1, allows the receiver to be rotated past the specimen independent of the transmitter, hence allowing the measurement of the intensity of scattered ultrasound across the sample. Figures 2-1, 2-2, and 2-3 show the three degrees of freedom and their characteristic motions.



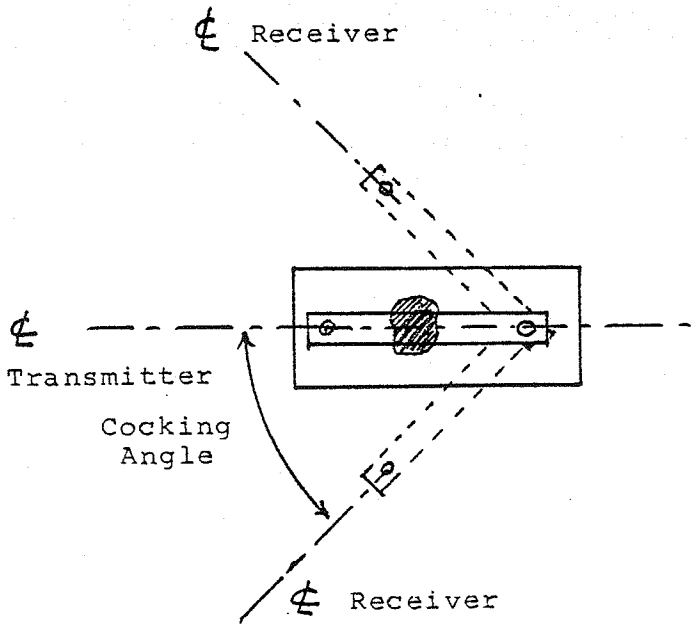
Transmitter and receiver rotate about specimen

Fig. 2-1 Rotational Degree of Freedom



Centerline of transmitter and receiver sweep through specimen

Fig. 2-2 Typical 90 Degree Fan-Beam Sweep



Centerline of receiver moves
Centerline of transmitter remains stationary

Fig. 2-3 Cocking Degree of Freedom

Throughout the conception, design, and construction of the scanner, an effort has been made to be compatible with the Mayo scanner. The mechanics of the scanner constitute an improvement over the Mayo Clinic implementation. Mayo's scanner used stepping motors. Special driving circuitry had to be designed to alleviate vibrational problems. In the UCAT at the Bioacoustic Research Laboratory, DC servomotors are used to drive each degree of freedom with continuous smooth motion. A control scheme had to be devised to provide positional and velocity control of the various degrees of freedom and to direct the acquisition of data during the fan-beam sweep.

2.2 Overall System Design

Control of the various degrees of freedom presents a formidable task when a pure hardware implementation is considered. A SYM-1 microprocessor board, by Synertek, was specified by Lerner (1979) as a method of distributing a software resident control algorithm among the three degrees of freedom. Microprocessor control takes a significant load off of the Interdata allowing it to service the DAS and gather the scan data taken during the scan. A microprocessor also provides upwards compatability with any mechanical changes that may be incorporated into the system in the future.

A separate controller system bus was designed to communicate between the SYM-1 and the hardware elements that make up the control system. The control system hardware must provide a means of controlling the speed and direction of each motor and reading the position of each of the degrees of freedom. Positional feedback is provided by optical encoders. The implementation of the optical encoders requires that the control system software be able to determine when the encoders are initialized. Interrupts must be provided to tell the Interdata computer to take data. A provision is made to allow rough positional control, independent of the SYM, via a hand held manual control box. This permits manual initialization of the optical encoders. A block diagram of

the interconnections between the Interdata, the SYM, and the scanner control hardware is provided in figure 2-4.

The following chapter will describe the SYM-1 microcomputer and the circuitry required to interface the SYM-1 with the scanner controller bus. Chapter 4 will describe the control hardware elements on a card-by-card basis, discussing their purpose, design constraints, programming considerations, and, when applicable, relationship to the mechanics of the scanner.

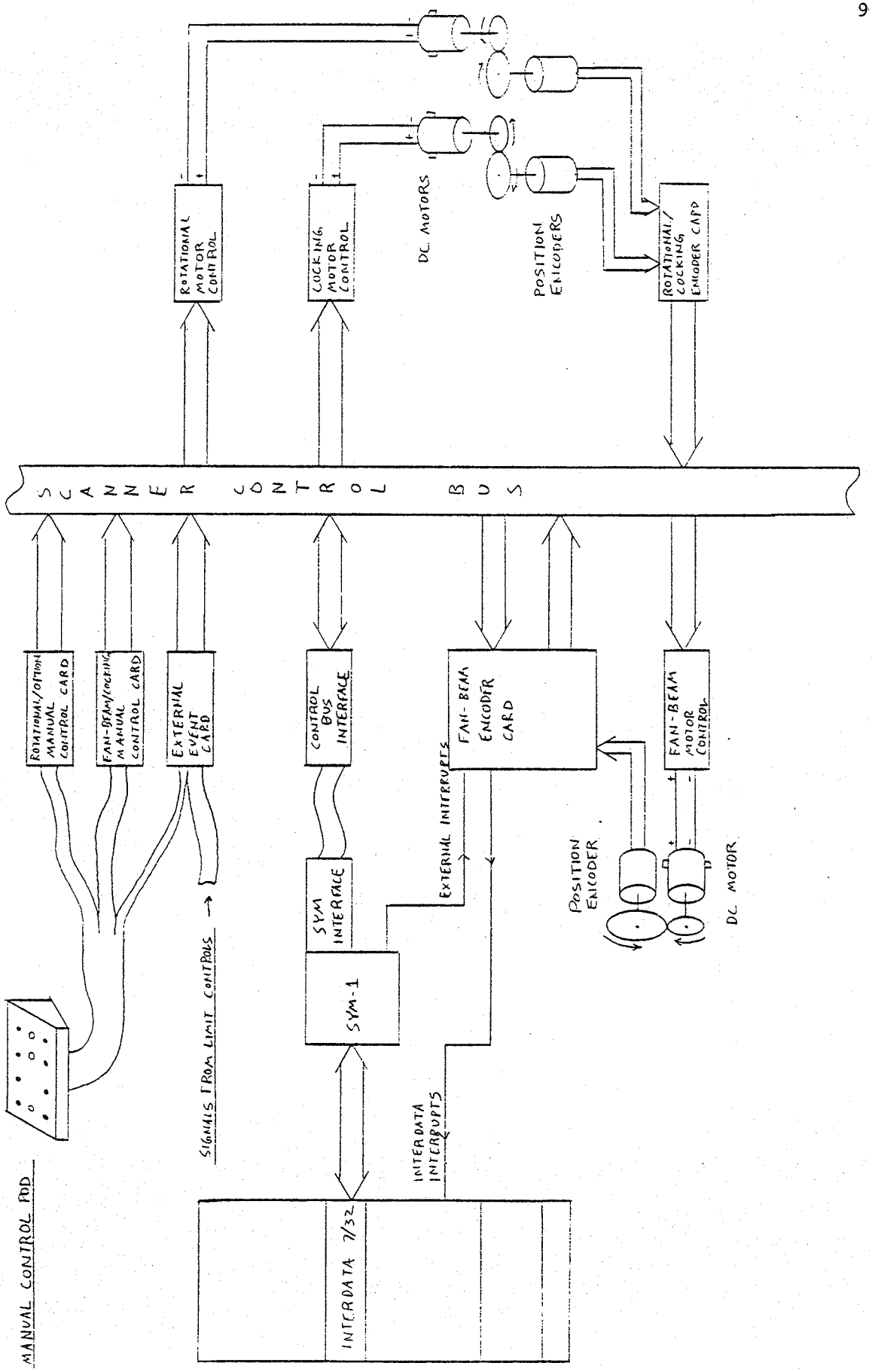


Fig. 2-4 Overall System Block Diagram

Chapter 3

Microcomputer Interface

3.1 The SYM-1 Microprocessor Board

3.1.1 Board Description

The SYM-1 board contains a 6502 microprocessor and all necessary support circuitry, including memory as well as parallel and serial ports. The SYM-1 comes equipped with 4K of on-board RAM and three expansion sockets for user application ROM. A system monitor, supplied with the SYM, resides in a 4K ROM. This monitor supports the 28 key keypad and 6 digit LED display mounted on the SYM-1 board, and allows the many monitor supported functions to be executed by user programs. A total of 71 active input-output lines as well as six interval timers are provided by the three 6522 Versatile Interface Adaptors (VIA's). Two 44-pin edge connectors accomodate the applications port and the auxiliary applications port, allowing access to the input/output lines of the 6522 ports.

An additional 44-pin edge connector known as the expansion port, provides access to the 6502 microprocessor bus and control signals. This port, normally used for expanding memory or adding external devices not present on the SYM-1 , is of primary importance in the scanner implementation. A

listing of the pins of the expansion port used in the scanner interface, and their functions, may be found in figure 3-1. For a complete listing refer to the SYM-1 Referance Manual page 4-7.

Bus Pin	Signal	Bus Pin	Signal
1		A	AB0
2		B	AB1
3		C	AB2
4		D	AB3
5		E	AB4
6		F	AB5
7	$\overline{RST}$	G	AB6
8	DB7	H	AB7
9	DB6	K	AB8
10	DB5	L	AB9
11	DB4	M	AB10
12	DB3	N	AB11
13	DB2	P	AB12
14	DB1	R	AB13
15	DB0	S	AB14
16		T	AB15
17		U	Ø2
18		V	R/$\overline{W}$
19		W	
20	RESET IN	X	
21	+5V	Y	
22	GND	Z	

Fig. 3-1 Pertinent Expansion Port Signal Lines

Signal lines AB0 - AB15 provide the 16 address lines needed to select the various elements of the control system hardware. Lines DB0 - DB7 provide a bidirectional data path to the microprocessor. Signal $\overline{RST}$ is the system reset line from the microprocessor, while RESET IN may be used to reset the microprocessor from the control system. The Ø2 system clock and R/$\overline{W}$ (read/(not)write) control line, when combined

in the appropriate manner tell a device whether to talk on the bus (send data to the CPU) or to listen to the bus (receive data from the CPU). These are the two signals from which the read strobe and write strobe are created.

3.1.2 General Memory Map of the SYM-1

The SYM-1 has many devices attached to its bus, all of which are memory mapped. When designing around the existent devices it is important to realize which memory locations are already used, which locations will be used in the future, and which addresses will never be used. An overall memory map of the SYM-1 address space may be seen in figure 3-2.

Each VIA has a set of addresses, each address having a unique function. Since the VIA functions are not used in the scanner control hardware, it is beyond the scope of this presentation to discuss all of the VIA capabilities. For a detailed discussion of the functional memory map of the VIA's, pages 4-19 through 4-25 of the SYM-1 Reference Manual should be consulted.

Function	Address Starting	Ending
Interrupt Vectors	FF80H	FFFFH
Unused	E000H	FF7FH
Future Expansion	C000H	DFFFH
Unused	B000H	BFFFH
VIA #3	AC00H	AFFFH
VIA #2	A800H	ABFFH
System RAM - 6532	A600H	A7FFH
System I/O - 6532	A400H	A5FFH
VIA #1	A000H	A3FFH
Future Monitor Expansion Area	9000H	9FFFH
4K Supermon Monitor	8000H	8FFFH
Scanner Control Hardware	7FF0H	7FFFH
Unused	1000H	7FEFH
3K User RAM	0400H	0FFFH
512 Byte User RAM	0200H	03FFH
System Stack	0100H	01FFH
Page Zero	0000H	00FFH

Fig. 3-2 SYM-1 General Memory Map

3.1.3 Scanner Contol System Memory Map

The scanner control system contains many elements, each of which occupy one or more memory addresses between 7FF0H and 7FFFH. The individual circuits that make up the control system, their functions, and individual memory maps will be presented on a board-by-board basis in Chapter 4. It was thought, however, that an overall scanner control system memory map may be helpful as a programming guide as well as a general reference. Figure 3-3 shows the memory locations and their functions, for both read and write operations, as they pertain to the scanner operation. Additional information, including programming considerations and suggestions, on the functions of the control system hardware

is available in Chapter 4.

Write Function	Address	Read Function
Fan-Beam Speed	7FF0H	Limit Status Byte
Fan-Beam Direction	7FF1H	Unused
Cocking Speed	7FF2H	Unused
Cocking Direction	7FF3H	Unused
Rotational Speed	7FF4H	Unused
Rotational Direction	7FF5H	Unused
-Reserved-	7FF6H	Unused
-Reserved-	7FF7H	Unused
Positional Interrupt Register LO	7FF8H	Fan Beam Encoder LO
Positional Interrupt Register HI	7FF9H	Fan Beam Encoder HI
Positional Interrupt Disable	7FFAH	Cocking Encoder LO
Unused	7FFBH	Cocking Encoder HI
Unused	7FFCH	Rotational Encoder LO
Unused	7FFDH	Rotational Encoder HI
Reset Interrupt/ Passed-Zero Status	7FFEH	Passed-Zero/ Interrupt Status
Unused	7FFFH	Unused

Fig. 3-3 Scanner Control Hardware Memory Map

Since one cannot readily determine which functions reside on which circuit boards, a cross reference list is presented in figure 3-4.

Function	Circuit
Speed and Direction	Pulse Width Modulator Board (Sec 4.1.1)
Limit Status Byte	External Event Board (Sec 4.3.1)
Fan-Beam Encoder Positional Interrupt Register Positional Interrupt Disable Reset INT/Passed Zero Flags	Fan-Beam Encoder Board (Sec 4.2.3)
Cocking Encoder Rotational Encoder Passed Zero Flags/INT Status	Rotational/Cocking Encoder Board (Sec 4.2.4)

Fig. 3-4 Function/Circuit Cross Reference Listing

3.1.4 SYM-1 Interface Card

3.1.4.1 Device Description

Before a control system bus can be defined, it is necessary to isolate the appropriate lines at the SYM-1 expansion port. Address decoding must be provided for the high order 12 address bits and bidirectional buffering must be supplied to enable the system data bus to be brought off of the SYM-1 board. These bidirectional buffers, known as bus transceivers, must be enabled to transfer data in the appropriate direction at the appropriate time. In addition, all control signals must be buffered to prevent extensive bus loading and protect the sensitive CMOS circuitry on the SYM-1 board. The logic on the SYM-1 Interface Card serves all of these functions and provides a 40-conductor ribbon cable

connector to interconnect with the Control System Interface Card.

3.1.4.2 Circuit Description

The SYM-1 Interface Card is directly mounted on the expansion port of the SYM-1 microcomputer and it derives its power from the +5 volts and ground supplied on pins 21 and 22 of the expansion port connector. A circuit diagram for this interface is provided in figure 3-5.

High order address decoding is accomplished by 8-input NAND gate IC3 and inverter IC9a. If the high order address byte is 7FH, the output of IC3 goes low. Address bits A7 through A4 are decoded by NAND gate IC8. If all ones are presented to the inputs, the output of IC8 goes low. This output, as well as the output of IC3 are AND'ed together by IC9b to form address enable line 7FFX. As long as the 12 high order address bits are 7FFH, the enable line will be high. This line then proceeds on to the Control System Interface Card via the 40-conductor ribbon cable.

The low order four address bits pass through 4-bit latch IC2 and then onto the Control System Interface Card. IC2 latches the address bits on the rising edge of Ø2 (the beginning of each machine cycle). This extends the time that the address is available to the control system circuitry.

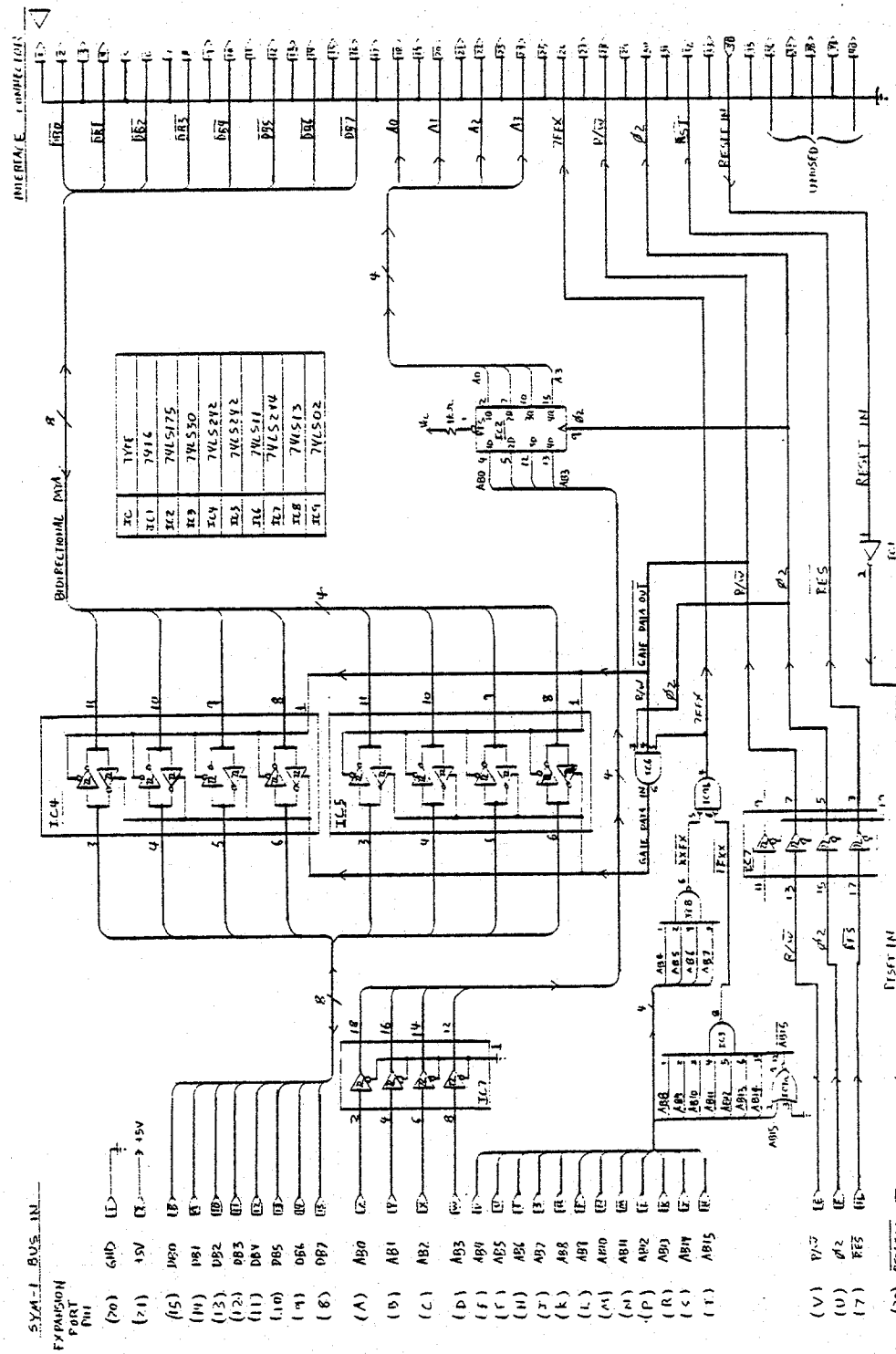


Fig. 3-5 SYM Interface Card Circuit Diagram

Bidirectional bus drivers IC4 and IC5 buffer the SYM-1 data bus and transmit data to and receive data from the Control System Interface Card. At the SYM-1 end of the interface, it is important that the bus drivers not output onto the SYM-1 bus unless a read cycle is entered and the address bus is accessing the scanner control hardware (the 7FFX line is high). During a read cycle, the 6502 processor expects valid data on its bus at the falling edge of Ø2. The timing diagram in figure 3-6 shows the state of the control lines

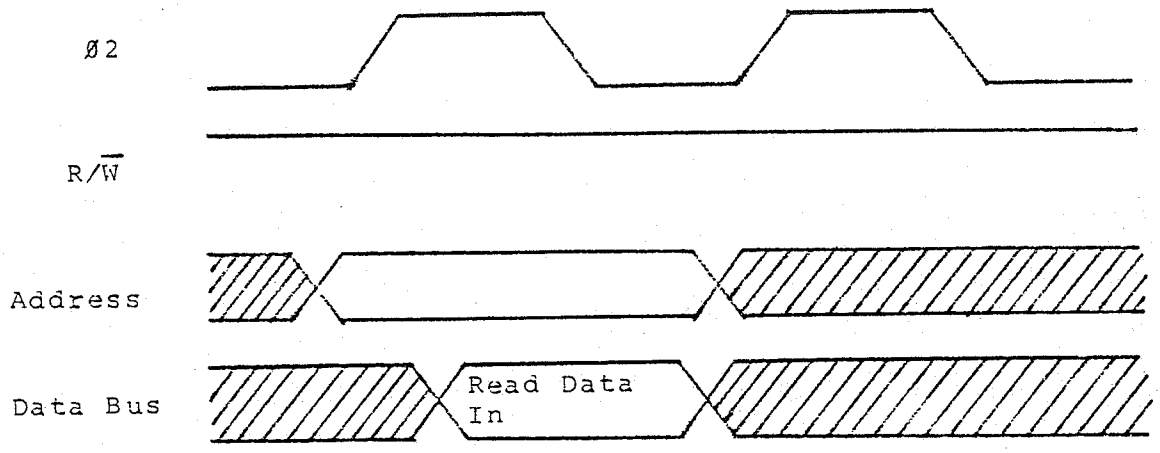


Fig. 3-6 6502 Microprocessor Read Timing Diagram

and data bus during a read cycle of the 6502 CPU. AND gate IC2 requires that the address bus read 7FFXH, that Ø2 be high, and the R/$\overline{W}$ line be high. When all of these conditions are satisfied, the bus transceivers are enabled to present data, coming from the control bus, to the SYM-1 data bus.

The system must only write to the SYM-1 bus at the appropriate time, however it may always read the SYM-1 bus. A line is provided from R/$\overline{W}$ to enable IC4 and IC5 such that when the SYM-1 wishes to write data (R/$\overline{W}$ goes low), it is always transferred to the Control System Interface Card, regardless of the address being written to. The Control System Interface Card always sends this data to the Controller Bus, however, it does not always send a strobe to latch the data. More information on the operation of the Control System Interface is contained in section 3.1.5.

Buffering for address lines A0 through A3 and SYM-1 control lines is provided by IC7. Open collector driver IC1 allows the Control System Interface Card to reset the SYM. The 40-conductor cable carrying the data, address, and control signals, has interlaced ground conductors to reduce crosstalk and induced noise.

3.1.5 Control System Interface Card

3.1.5.1 Device Description

The Control System Interface accepts signals sent from the SYM-1 Interface Card and forwards them onto the controller bus at the appropriate time. Bus transceivers are used to communicate between the SYM-1 Interface Card and the controller data bus. This circuit decodes the SYM-1 control signals and synthesizes a read strobe ($\overline{RDSTB}$) and write

strobe ($\overline{WRSTB}$) to allow reading and writing to the control hardware elements. Address lines A0 through A3 specify which device is to be written to or read from. Hence, the Control System Interface actually defines the controller bus.

A provision is made for selection of automatic operation or manual operation of the control system. The AUTO/$\overline{MAN}$ mode select line is controlled by a toggle switch located on the Manual Control Pod and wired through the External Event Card to the controller bus. When manual mode is entered, the control bus interface allows its bus drivers to float the data bus, address bus, and control signals, thereby permitting the Manual Control Boards to take control of the bus.

The system clock that drives the Pulse Width Modulator is also located on the Control System Interface. This clock drives various cascaded counters and other incidental logic to provide the timing signals necessary for the operation of the Manual Control Boards.

3.1.5.2 Circuit Description

The Control System Interface Card plugs into the controller bus providing the link between the control system bus and the SYM-1 Interface Card. A diagram of this circuit is provided in figure 3-7. This circuit derives its power from the control system bus power lines. The interface cable from the

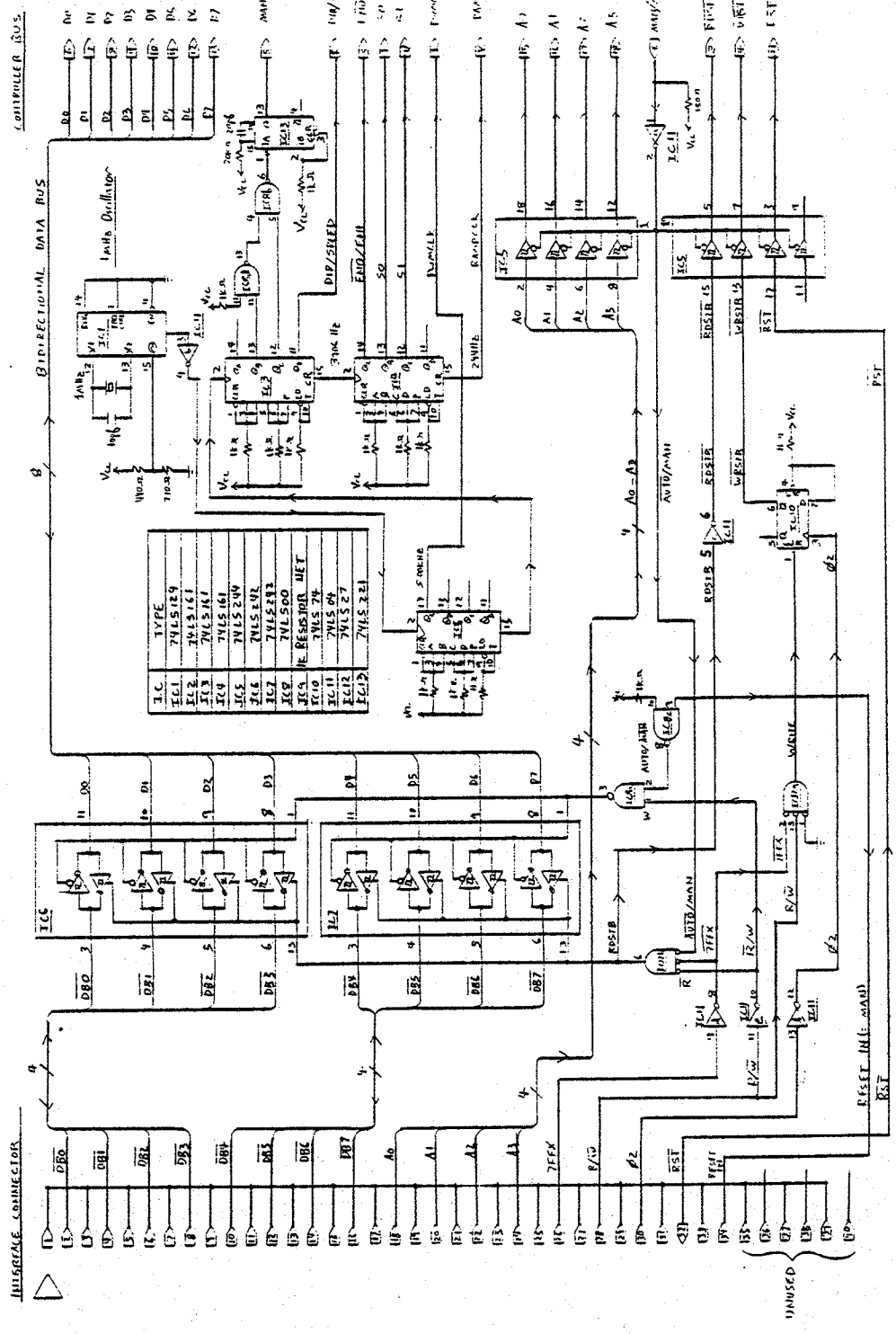


Fig. 3-7 Control System Interface Circuit Diagram

SYM-1 Interface Card has interlaced grounds, but they are only connected to the ground on the SYM-1. By maintaining only one ground connection, ground loop problems associated with multiple ground paths are eliminated.

The low order address bits A0 through A3 pass from the interface cable to bus driver IC5 and then onto the controller bus Each circuit card plugged into the controller has its own address decoder which compares A0 - A3 with its preset address. When an address match occurs, read or write operations may take place dependent upon the state of the read or write strobe. A read operation will occur when $\overline{\text{RDSTB}}$ is asserted low, while write operations occur on the falling edge of $\overline{\text{WRSTB}}$. No data will be read from or written to the scanner control hardware unless the $\overline{\text{RDSTB}}$ or $\overline{\text{WRSTB}}$ strobes are present.

The Control System Interface accepts and sends data to the SYM-1 Interface Card via bidirectional bus drivers IC6 and IC7. Since the SYM-1 Interface Card accepts data only when R/$\overline{W}$, Ø2, and 7FFX are high, IC12b is provided to enable bus drivers IC6 and IC7 to send data present on the controller bus out to the SYM. IC12b also provides the $\overline{RDSTB}$ signal to the control bus by way of inverter IC10c. Only when a read cycle is in progress (R/$\overline{W}$ is high), the control system is being accessed on the address bus (7FFX is high), and the system is in automatic mode, will IC12b cause $\overline{RDSTB}$ to go low and enable bus drivers IC6 and IC7 to put data out to the SYM-1 interface. The data is present at the SYM-1 interface before it is needed by the SYM-1 interface bus drivers. This early arrival of data allows time for the signals to settle on the interface connector cable. A timing diagram for the complete read operation is provided in figure 3-8.

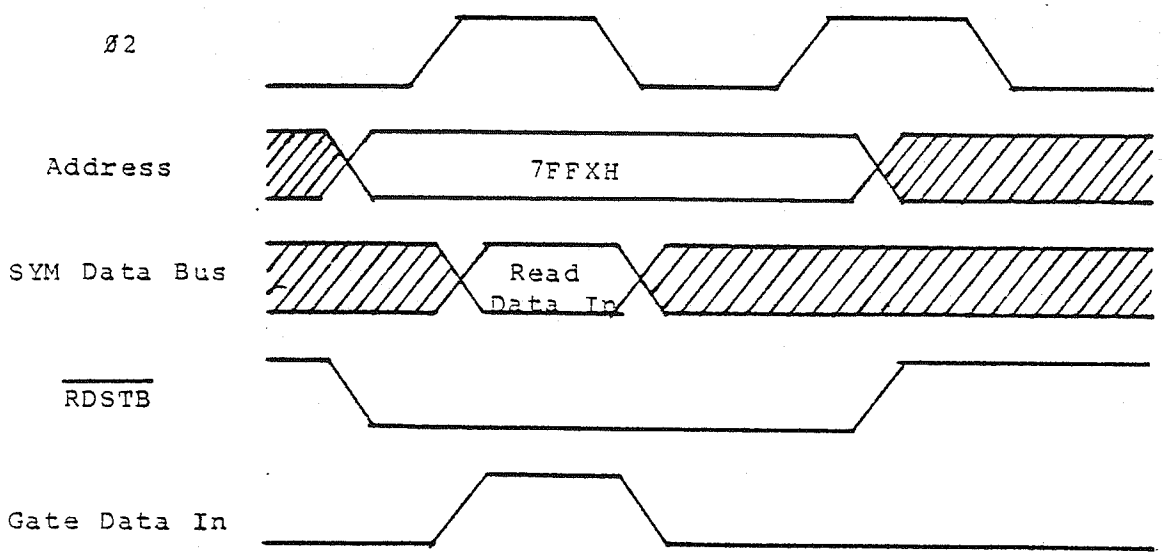


Fig. 3-8 Control System Read Cycle Timing Diagram

The timing involved for the write cycle is more critical than the read operation primarily because the write operation is edge triggered. From the control system write cycle timing diagram in figure 3-9, it can be seen that data must be latched by the addressed board on the falling edge of Ø2 during the write cycle (R/$\overline{W}$ low).

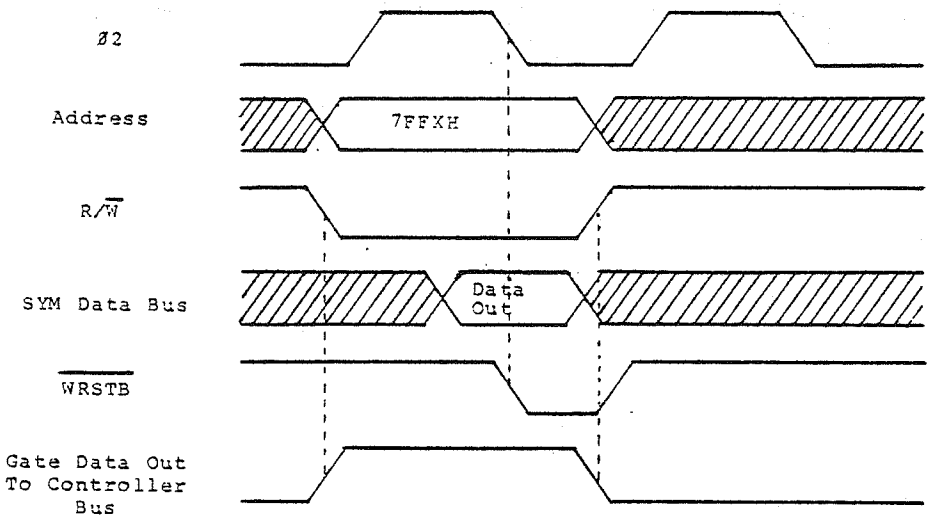


Fig. 3-9 Control System Write Cycle Timing Diagram

For the duration of the write cycle, data from the SYM-1 is allowed to pass through the interface cards to the control system bus (if the system is in automatic mode) via IC6 and IC7 enabled by IC8a. By enabling data to pass well in advance of the $\overline{\text{WRSTB}}$ signal, the data has time to settle on the control bus. This satisfies the setup time required by the latches storing the data in the individual control hardware circuits. While IC8a enables data to pass to the controller bus, IC12a and IC10 work together to provide the WRSTB signal. Flip-flop IC10 is normally held cleared by IC11a. When a write operation is being performed ($R/\overline{W}$ is low) and the control system is being addressed ($\overline{7FFXH}$ is low)

IC12a removes the clear and allows a logical 1 at the D input to be clocked into IC10 by the rising edge of Ø2. At the end of the write cycle R/$\overline{W}$ goes high and the clear state is again entered. The inverted output of the flip-flop, $\overline{Q}$, becomes the signal $\overline{WRSTB}$.

Automatic mode allows the SYM-1 to take control of the controller bus while manual mode relinquishes the bus to the Manual Control Boards by floating the data bus via IC8a and IC11b. Manual mode also floats the address bus and all control signals on the controller bus by disabling tristate bus driver IC5. IC10a and IC8c provide buffering, so as to present only one LS-TTL load to the AUTO/$\overline{MAN}$ signal line, as well as level inversion for the disabling of the bus drivers.

A 1 MHz crystal oscillator (IC1) is provided as the system clock. This clock is divided down by counter IC2 to form the 500 KHz pulse width modulator clock. Additional counters IC3 and IC4, AND gates IC8b and IC8d, and one-shot IC13 produce the necessary timing signals required by the Manual Control Boards. These signals are only used by the Manual Control Boards and hence will not be discussed in this section. For a detailed treatment of the signal functions and uses, refer to the section on the Manual Control Card (Sec 4.4.1).

3.1.5.3 Control Bus Description

The transformation from the SYM-1 bus to the control system bus is completed in two circuit boards (the SYM-1 Interface connected to the Control System Interface). Though most of the signals on the bus are produced by the Control System Interface, some signals are produced on the different boards that make up the control system. The following description presents each signal of the controller bus on a pin-by-pin basis. Points of origin for each signal are noted as well as areas in which the signals are used. For detailed information on the signals and their use refer to the individual circuit descriptions of the control system hardware.

Pin- 1 PWMCLK - This is a 500 KHz square wave generated by the Control System Interface and used by each Pulse Width Modulator card to generate fixed frequency pulses of variable width.

Pin- 2 +8V - This is an unregulated 8 volt source sent to each optical encoder via their respective encoder interface card. This voltage is regulated to +5 volts at the open-collector buffer and regulator circuit attached to each encoder.

Pin- 3 $\overline{\text{RDSTB}}$ - Generated by the Control Bus Interface card, this signal is used to strobe data out of any card that supports a read operation.

Pin- 4 $\overline{\text{WRSTB}}$ - The write strobe, produced in the Control System Interface circuit, causes any circuit that supports a write operation to latch the data present on the controller data bus. Latching occurs on the falling edge of $\overline{\text{WRSTB}}$.

Pin- 5 MANWRSTB - Manual write strobe is a signal generated on the Control System Interface card and used by the Manual Control Boards to write speed and direction data to the Pulse Width Modulator cards.

Pins 6-13 D0 - D7 comprise the bidirectional data bus. The port of entry and exit of these signals is the Control System Interface, however these signals are used by any circuit that has the ability to be read from or written to. Manual Control generates D0 - D7 to control the motors by way of the Pulse Width Modulators, when in manual mode.

Pin-14 Unused

Pins 15-18 A0 - A3 comprise the controller address bus. In automatic mode - generated at the Control System Interface, in manual mode - generated at the Manual Control Boards, these signals specify which address is being read from or written to.

Pin-19 ZFANBEAM - Generated by the fan beam encoder and brought out to the controller bus by the Fan-Beam Encoder Card, this signal sets the fan-passed-zero flip-flop on the Rotational/Cocking Encoder Card.

Pin-20 $\overline{\text{IFRST}}$ - This signal, produced on the Fan-Beam Encoder Card is brought low when address 7FFEH is written into or a reset is generated at the SYM. $\overline{\text{IFRST}}$ resets the Interdata interrupt flip-flop on the Fan-Beam Encoder Card and resets all passed-zero flip-flops on the Rotational/Cocking Encoder Card.

Pin-21 $\overline{\text{RST}}$ - The reset signal used by most all boards (except Manual Control) to reset all states to zero.

Pin-22 Reserved - If a board were inserted

upside down, +5V would be tied to this line. This pin remains unused to prevent possible circuit damage.

Pin-A GND - Power ground is wired directly to the power supply and used by all boards plugged into the controller bus.

Pin-B INTERDATA INTERRUPT - This output signal goes high to cause an interrupt at the Interdata minicomputer. It is generated on the Fan Beam Encoder Card and is used to direct data collection by the Interdata at regular intervals during a fan beam sweep. Interrupts may also be caused by the EXT INT line.

Pin-C EXT INT - This input line, used to provide an external means of producing interrupts to the Interdata, passes through the Fan-Beam Encoder Card to form the INTERDATA INTERRUPT signal.

Pin-D ZPF - Generated on the Rotational/Cocking Encoder Card, this open-collector signal normally grounds out the anode of a fan-beam passed zero indicator LED. When the fan-beam encoder passes through zero, the ZPF line goes high permitting

illumination of the LED. This indicates that the fan-beam encoder circuitry is initialized. This signal, passed through the appropriate manual control card, illuminates the right most LED on the Manual Control Pod.

Pin-E AUTO/$\overline{\text{MAN}}$ - Supplied by a switch on the Manual Control Pod, this signal passes through the External Event Board to the controller bus. The signal is used by the Control System Interface to disable the bus signals allowing the Manual Control Cards to take over the bus. The Manual Control Cards are enabled by this signal.

Pin-F RCWLIM - Rotational clockwise limit, provided by an opto-interrupter, through the External Event Card, to limit the clockwise motion of the rotational degree degree of freedom. This signal is used by the Pulse Width Modulator to terminate clockwise motion of the rotational degree of freedom.

Pin-H RCCWLIM - Same as RCWLIM except this signal limits countercockwise rotation of

the rotational degree of freedom.

Pin-J CKCWLIM - Same as RCWLIM except this signal limits clockwise motion of the cocking degree of freedom.

Pin-K CKCCWLIM - Same as CKCWLIM except this signal limits the counterclockwise motion of the cocking degree of freedom.

Pin-L FBCWLIM - Same as RCWLIM except this signal limits clockwise motion of the fan-beam degree of freedom.

Pin-M FBCCWLIM - Same as FBCWLIM except this signal limits counterclockwise motion of the fan-beam degree of freedom.

Pins N, P Unused limit control lines, provided to accomodate a future fourth degree of freedom.

Pin-R DIR/$\overline{\text{SPEED}}$ - A continuous square wave , produced on the Control System Interface Card and used to control when the Manual Control Card writes direction or speed information to the Pulse Width Modulator.

Pin-S $\overline{\text{EN0}}$/EN1 - This signal, generated on the Control System Interface Card, is used to

control which Pulse Width Modulator is being addressed by the Manual Control Card.

Pins T, U — S0, S1 - These signals, produced on the Control System Interface Card, are used to enable up to four Manual Control Boards at the appropriate time.

Pin-V — RAMPCLK - A 244 Hz square wave is generated at the Control System Interface; this signal is used to drive the velocity ramp generators on the Manual Control Cards.

Pin-W — ZPC - Same as Pin D (ZPF) except this pin indicates the passage of the cocking degree of freedom through zero by illuminating the next-to-rightmost LED on the Manual Control Pod.

Pin-X — ZPR - Same as Pin D (ZPF) except this pin indicates the passage of the rotational degree of freedom through zero by illuminating the leftmost LED on the Manual Control Pod.

Pin-Y — Reserved - If a board were inserted upside down, the +8 volt supply would be

tied to this line. This pin remains unused to prevent possible circuit damage.

Pin-Z +5V - This is the +5 volt system supply, wired directly to the power supply and used by all circuits plugged into the controller bus.

Chapter 4

System Components

4.1 Motor Control Circuitry

Early on in the scanner design it was determined that DC motors would be required to drive the three degrees of freedom. The advantage of using a DC motor in this application was documented in the first implementation of the scanner designed with stepping motors at The Mayo Clinic. It was demonstrated that stepping motors introduced mechanical noise that was picked up by the receiving element.

In controlling the speed and direction of a DC servo motor by microprocessor, it is necessary to control the polarity and magnitude of the voltage applied to motor armature. In the first implementation of a control scheme, implemented by Lerner (1979), the concept of pulse width modulated motor control was presented. Each degree of freedom to be controlled requires a Pulse Width Modulator Card and a Motor Power Driver Card. The following sections describe the implementation of pulse width modulated control.

4.1.1 Pulse Width Modulator Card

4.1.1.1 Device Description

The Pulse Width Modulator (PWM) Card provides signals to the Motor Power Driver Card to turn on and turn off the power to the motor at a fixed repetition rate, the pulse width being proportional to the value stored in the motor speed byte. This value can vary from 00H (no voltage at all) to FFH (full voltage). The PWM may reverse the polarity of the voltage being supplied to the motor to reverse its direction. The polarity reversal is controlled by two direction bits within the direction byte. Because direction and speed are latched, it is possible to have simultaneous motion of all three degrees of freedom.

The concept of pulse width modulation is advantageous because the driver transistors of the Motor Power Driver Circuitry are either saturated or cutoff, thus minimizing power dissipation. Had an approach been taken using a D/A converter with a linear amplifier, the transistors of the amplifier would be in the active region most of the time and hence, the power dissipated would be greater.

The address of the speed byte and direction byte within the control system memory space may be varied by DIP switch selection. Possible address settings are listed in figure 4-1.

Address	Function	Switch Pos 1	2	3
7FF0H	Speed	C	C	C
7FF1H	Direction			
7FF2H	Speed	C	C	O
7FF3H	Direction			
7FF4H	Speed	C	O	C
7FF5H	Direction			
7FF6H	Speed	C	O	O
7FF7H	Direction			
7FF8H	Speed	O	C	C
7FF9H	Direction			
7FFAH	Speed	O	C	O
7FFBH	Direction			
7FFCH	Speed	O	O	C
7FFDH	Direction			
7FFEH	Speed	O	O	O

NOTE: O = Switch open (OFF), C = Switch closed (ON)

Fig. 4-1 PWM Address Selector Settings

Hence, it is possible to configure each motor into one of 8 memory spaces. Care should be taken to set the motor address such that other write addressed devices do not occupy the same address. The present system configuration specifies the locations for each of the PWM addresses. A memory map of these addresses is presented in figure 4-2.

Address	Function	Degree of Freedom
7FF0H	Speed	Fan-Beam
7FF1H	Direction	Fan-Beam
7FF2H	Speed	Cocking
7FF3H	Direction	Cocking
7FF4H	Speed	Base Rotation
7FF5H	Direction	Base Rotation
7FF6H	Speed	Future Degree
7FF7H	Direction	Future Degree

Fig. 4-2 System PWM Memory Map

4.1.1.2 Programming Considerations

The PWM Card has two control registers, one for speed and one for direction. The speed control register contains an 8-bit value specifying one of the 256 possible pulse widths (voltages) to be sent to the motor. Of the 8 bits that may be written to the direction register, only the low order two bits have meaning. The four possible states of the direction bits and their functions are outlined in figure 4-3, below.

Bit 0	Bit 1	Action
0	0	Stop
0	1	Forward
1	0	Reverse
1	1	Stop

Fig. 4-3 Direction Register Bits and Associated Functions

It is suggested that the speed control register be loaded first; in doing this sudden direction changes at full speed will be avoided. The addresses of the control registers and

the motors they control are outlined in the previous figure 4-2.

The directions of rotation of the degrees of freedom as controlled by the direction control register, are dependent upon the gearing from the motor to the degree of freedom in question. Figure 4-4 serves as a quick reference in determining which degrees of freedom are moved in which direction by the respective bits of the direction byte.

Degree of Freedom	Direction Byte Bit 0 = 1 Bit 1 = 0	 Bit 0 = 0 Bit 1 = 1
Fan-Beam	CW	CCW
Cocking	CCW	CW
Base Rotation	CCW	CW

Fig. 4-4 Direction Bit Meanings

A motor controlling a degree of freedom will continue in the specified direction and speed until its limit control is tripped. When this occurs, the motor will only be able to move in a direction opposite the direction in which it was moving that caused the limit condition. A system reset will set the speed control register to zero and set the direction control register to zero.

4.1.1.3 Circuit Description

The PWM Board consists of a pulse width generator, a delay

generator, output drivers, an address decoder, and various additional logic. A circuit diagram is shown in figure 4-5.

The pulse width generator is composed of two free running 4-bit counters IC13 and IC14, two magnitude comparators IC1 and IC2, and an 8-bit speed control register IC7. The comparators continually compare the speed control register contents with the value of the free running counters. As long as the counter value is less than the value stored in the speed control register (the speed control byte), pin 5 of IC2 remains high. This output could be used as the pulse width modulated output. However, for the speed control value of FFH there will be a time, just before the counter overflows to 00H, where the counter value will not be less than the speed control register value. In simple terms, this prevents the motor from receiving full power supply voltage for the maximum possible speed control byte value. To prevent this occurence, if the high order bit of the speed byte is high (the value of the speed byte is greater than 80H) IC3a and IC10c change the pulse width modulator output to be brought high when the counter value is less than or equal to the value contained in the speed control register. This signal, indicated as PWM in the circuit diagram, goes on to the delay generator to form the pulse width modulated output signal to the Motor Power Driver Boards.

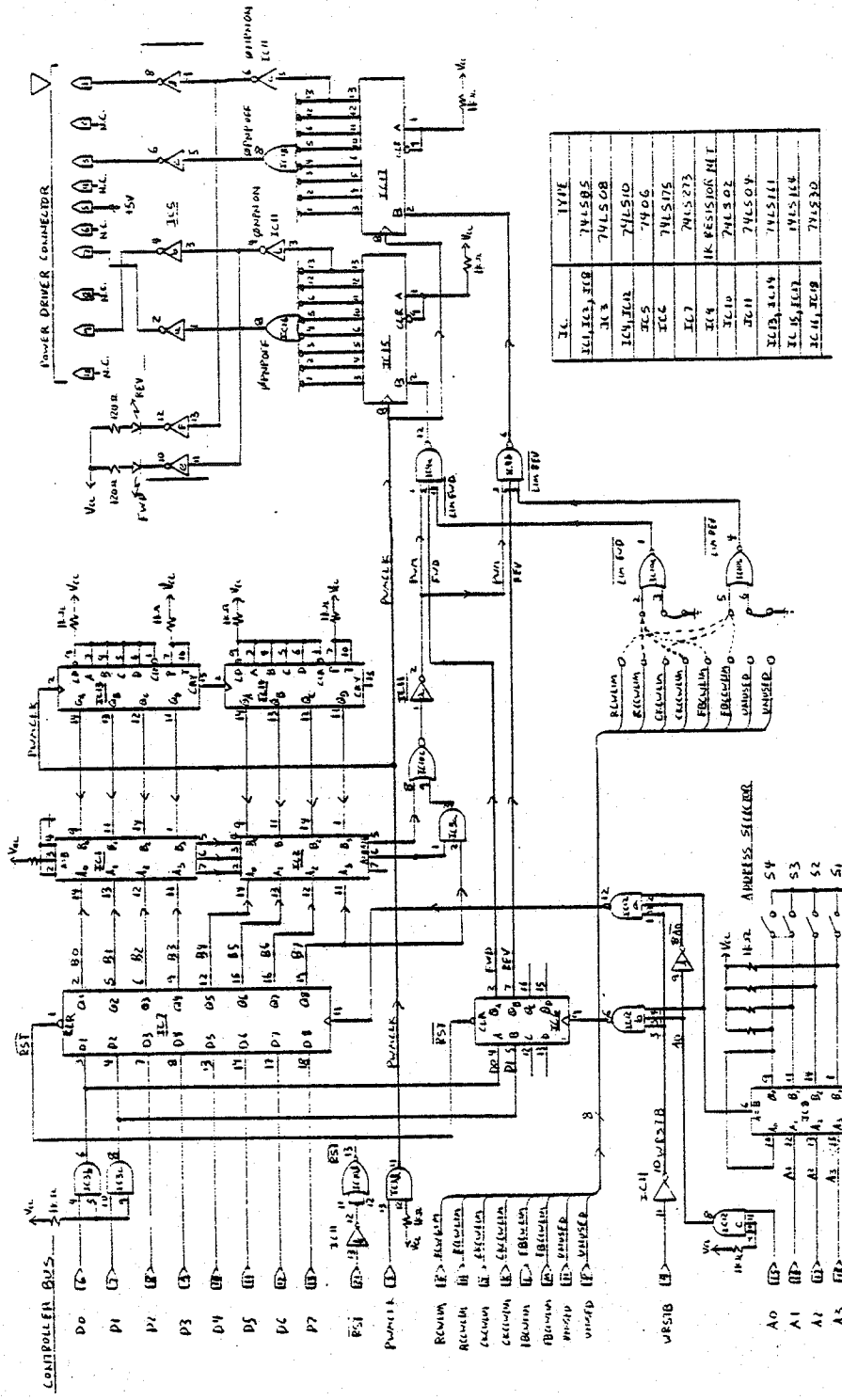


Fig. 4-5 Pulse Width Modulator Circuit Diagram

The delay generator allows time for the PNP transistors in the motor power driver to turn off before the NPN transistors are turned on. If both transistors were allowed to conduct at the same time, a momentary rail-to-rail short would occur across the motor power supply. For a detailed description of the Motor Power Driver circuit see Section 4.1.2.

The PWM line is fed through IC4a and IC4b to the 8-bit shift registers IC14 and IC17. The outputs of the shift registers are sent on to the 8-input NAND gates IC16 and IC18 as well as inverters IC11b and IC11c. If the appropriate direction control register bit is active (FWD or REV) and a limit condition does not exist, the PWM wave form will be fed into the shift register. The shift registers are clocked regularly by the 500 KHz PWM clock, hence a delay of 16 microseconds exists between the signal presented to the input and the signal at the 8th bit. The delay is used to prevent ØNPNON from turning the NPN transistors on before ØPNPOFF has been high for less than 16 microseconds. These signals are carried to the motor power drivers by way of a 10-conductor ribbon cable.

The output drivers (IC5) provide open collector outputs to sink current and turn on the opto-isolator LED's, and hence the respective transistors, on the power driver board. These drivers also provide a current sink to turn on the indicator LED's on the PWM board. The indicator LED's appear

brightness modulated because of the visual persistance of the human eye and provide visual feedback of the contents of the speed and direction registers for the purpose of debugging.

The address decoder compares the value A1 - A3 with the DIP-switch address select setting. If comparator IC8 detects a match between the address bus and the DIP-switch settings, the A=B line goes high and gates the $\overline{\text{WRSTB}}$ signal through inverter IC11d and AND gate IC12a speed control register IC7 or the direction control register. Latching of data occurs on the falling edge of $\overline{\text{WRSTB}}$.

Incidental logic provides buffering so that each card input presents only one LS-TTL load to the controller bus. Limit controls are connected through OR gates IC10a and IC10b. See section 4.1.1.4 for detail on the implementation of limit controls. The reset line on the bus ($\overline{\text{RST}}$) is connected to the clear line of both the speed control register IC7 and the direction control register IC6. This allows the system to power up with all motors off.

4.1.1.4 Implementation of Limit Controls

The design philosophy behind the limit controls is to limit motion only in the direction which caused the limiting condition to occur. In this manner, the system may remove the limiting condition by rotating the affected degree of freedom in a direction opposite that which caused the limit

to occur. Eight lines are provided to carry limit information. These lines allow both clockwise (CW) and counterclockwise (CCW) limits to be detected on four degrees of freedom.

The following figure outlines the connections used for limiting clockwise and counterclockwise motion on the three degrees of freedom.

Degree of Freedom	CW Limit		CCW Limit	
	Bus Line	IC Input	Bus Line	IC Input
Fan-Beam	FBCWLIM	IC10a	FBCCWLIM	IC10b
Cocking	CKCWLIM	IC10b	CKCCWLIM	IC10a
Base Rotation	RCWLIM	IC10b	RCCWLIM	IC10a

Fig. 4-6 PWM Limit Input Connections

NOR gates are provided on the limit inputs because the limits of one degree of freedom may be affected by the limits of another degree of freedom. An example of this is the cocking and fan-beam limits. Cocking moves only the receiver, while fan-beam moves both the receiver and transmitter. Since receiver motion would cause a limiting condition to occur (inasmuch as the tank may prevent further motion of the receiver arm), it may be necessary to use one set of limit detectors for both degrees of freedom. It is conceivable that future mechanical implementations of the scanner may require two sets of limit controls to limit motion on one

degree of freedom. The NOR gates present on the PWM cards may be used for this purpose. If only one input to the NOR gate is used (the most common implementation), the unused input pin must be tied to ground.

4.1.2 Motor Power Driver Card

4.1.2.1 Device Description

The Motor Power Driver circuit uses high power complementary pair transistors to supply the motor with power from either end of the supply. The PWM Board turns the transistors on and off at a fixed frequency with a variable duty cycle, controllable from the microprocessor. The effective voltage reaching the motor is proportional to the duty cycle as specified by the speed control byte in the PWM Card. When no pulses are being received, the power driver board provides a dynamic braking action in the motor.

Optical isolation is provided on the power driver card to isolate and protect the controlling circuitry from the high motor driving voltages present on the driver board. The separate enclosure provided for the driving electronics, as well as the optical isolation, significantly decrease the effects of noise induced by high current pulses present on the driver cards.

4.1.2.2 Circuit Description

Pulse width modulated signals enter the motor driver by way of a 10-conductor cable. Of the 10 lines available, only 5 lines are used. These lines are the numbered connections in the Motor Power Driver Card circuit diagram shown in figure 4-7. Line 5 is tied to the +5 volt supply on the PWM board and is connected to the anode of each of the opto-isolator LED's via a 150 ohm current limiting resistor. When the PWM's open-collector driver sinks current from the LED cathode, the phototransistor within the isolator conducts. A 100K resistor is provided between the base and emitter of the phototransistor to speed up its operation.

Transistors Q9, Q10 and Q11, Q12 provide level translation as well as a stage of amplification. These transistors are biased to operate in the saturated region. Transistors Q5 and Q6 are PNP darlington transistors while Q7 and Q8 are the matched complementary pair NPN darlingtons. These transistors provide the current gain necessary to drive high power complementary pair transistors Q1, Q2 and Q3, Q4. Resistors from emitter to ground are provided on Q5, Q6 and Q7, Q8 to decrease the switching time. D1 and D2 are flyback diodes that provide a path for inductive breakdown voltage across the motor armature. D3 and D4 provide current paths for the back emf of the motor when the power is turned off and the motor is still spinning.

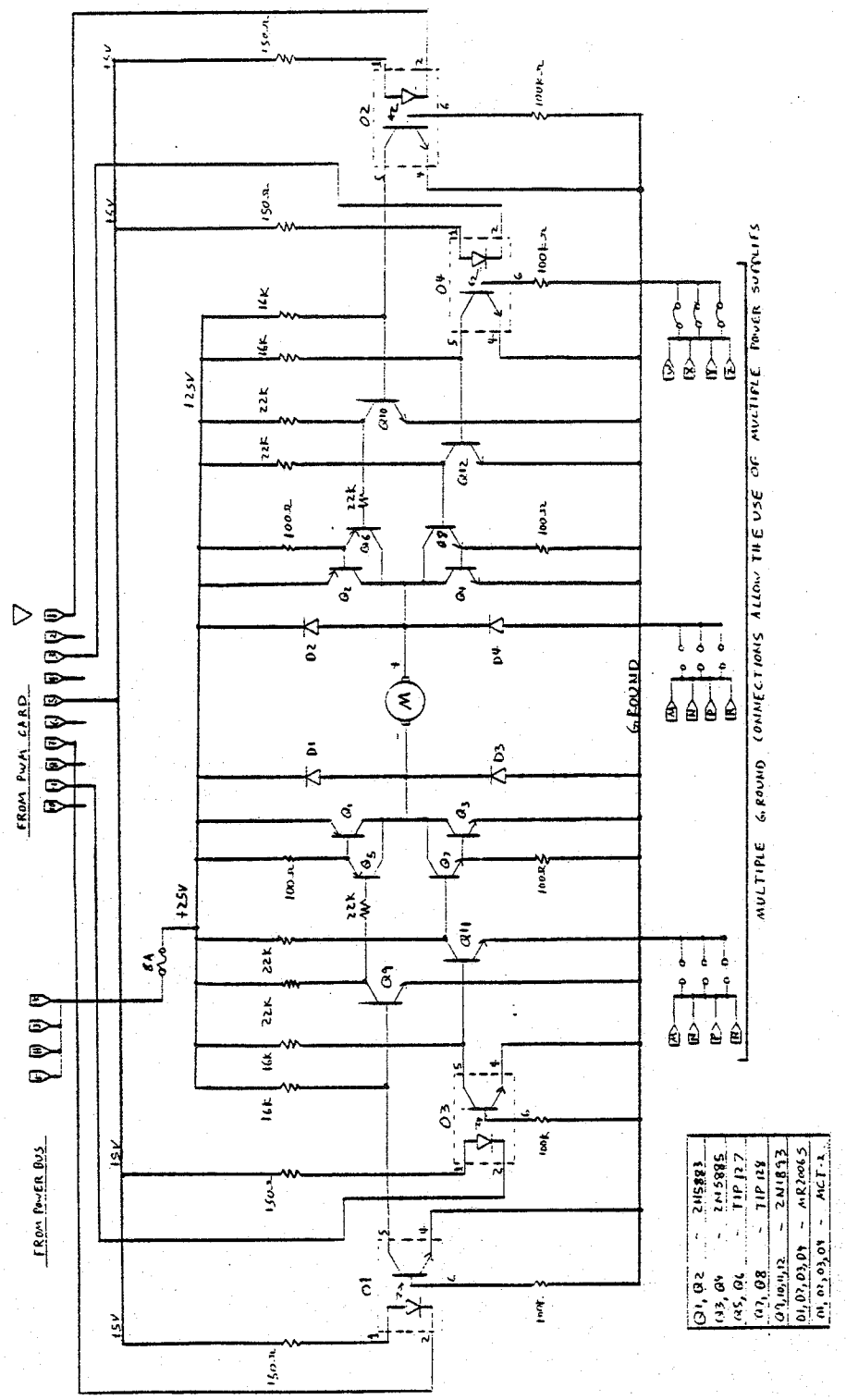


Fig. 4-7 Motor Power Driver Card Circuit Diagram

In the "stop" state, opto-isolators O1, O2 and O3, O4 are conducting. Transistors Q9, Q10 are cutoff by O1, O2 allowing the collectors to be pulled up by the positive supply rail. This cuts off the Q1, Q5 and Q2, Q6 pairs. Transistors Q11, Q12 are cutoff by O3, O4 allowing the Q3, Q7 and Q4, Q8 pairs to be forward biased by the 22K base resistor. If the motor is spinning in either direction a back emf is generated across the armature. This causes current to flow through D3 and Q4 or D4 and Q3 (dependent upon the direction of rotation). The mechanical energy of the spinning motor is converted to heat within the armature by resistive power dissipation; this provides a dynamic braking effect.

In the "forward" state, opto-isolators O1 and O3 remain saturated as in the "stop" state, however, opto-isolators O2 and O4 are cutoff. Transistor Q10 is forward biased in the saturated region, pulling the collector down to approximately ground potential; this forward biases the Q2; Q6 pair and ties the motor's positive lead to the positive motor supply voltage through Q2. The negative motor lead is tied to ground by Q3, as was outlined in the "off" state description. Since opto-isolator O4 is cutoff, Q12 is forward biased and pulls down the base of Q8 to ground, thereby cutting off the Q4, Q8 pair. This prevents a rail-to-rail short through Q2 and Q4.

In the "reverse" state, opto-isolators O2 and O4 remain saturated (as in the "stop" state) while O1 and O3 are cutoff. By the same mechanism as was described in the "forward" state, Q1 ties the negative motor lead to the positive motor supply voltage, while Q3 cuts off to prevent a rail- to-rail short. Q4 remains on and ties the positive motor lead to the ground rail. Hence, the polarity is reversed across the motor and rotation occurs in a direction opposite that of the "forward" state.

A fourth state exists in which both Q1 and Q2 are on while Q3 and Q4 are cutoff. This state is not used in the control system, however, its effect is the same as that of the "stop" state. Dependent upon the direction of motor rotation, either D1 and Q2 or D2 and Q1 provide a current path for the back emf developed across the spinning motor armature. Again, this provides a braking action.

The PWM signals switch between the forward and stop state or the reverse and stop state at a fixed frequency. The length of time in the forward or reverse state is directly proportional to the value in the speed control register. The direction control register determines whether the forward or reverse state is entered. The delay generator within the PWM Card provides a 16 microsecond delay between the turn-off of the PNP driver and the turn-on of the NPN driver, thereby allowing the PNP transistor to turn off completely before the

NPN transistor turns on and the stop state is entered.

4.2 Shaft Position Sensing

4.2.1 Optical Encoders

To control any shaft motion by a closed loop control system, a method of detecting the shaft position must be provided. The microprocessor must be able to read the shaft position of each of the three degrees of freedom. A device known as an optical encoder is employed to accomplish this task.

4.2.1.1 Device Description

An optical encoder consists of a shaft mounted transparent disk onto which precision markings have been etched. A beam of light is passed through the disk and is sensed by a photocell. As the shaft and disk assembly turn, the light beam is interrupted by the etched markings. The photocell output is sent to circuitry, within the optical encoder, that provides detection of the direction of rotation as well as uniform pulse widths of the signals, regardless of shaft speed. The encoders used in the scanner have three output signals: CCW, CW and ZREF. The CCW line is brought high every tenth of a degree of shaft rotation if the shaft is rotating in a counterclockwise direction. In the same manner, the CW line is asserted high every tenth of a degree of rotation if the shaft is rotating in a clockwise direction. Both the CCW and CW lines remain at logic low if

the shaft is not rotating. This type of encoder is called an "incremental" encoder and its resolution is said to be 10 ticks per degree or 3600 ticks per revolution. The ZREF line is pulsed high once for each rotation as the shaft of the encoder passes through the zero position. At all other times this line remains in a logic low state.

4.2.1.2 Circuit Description

The output lines of the encoder are standard TTL logic and break out into a DA15-P connector on the back of each encoder. The pins on this connector and their functions are listed in figure 4-8. Additional pins are provided on the connector to provide a case ground, signal ground, and entry point for the +5 volt supply required to power the encoder.

Function	DA15-P Pin Number
CW	13
CCW	14
ZREF	15
+5 V	6
GND	1
Case GND	9

Fig. 4-8 DA15-P Encoder Connector Pin Functions

4.2.2 Open Collector Buffer and Regulator Circuit

4.2.2.1 Device Description

As mentioned in the encoder circuit description, the encoders require a regulated source of +5 volts for power. In addition, the outputs of the encoder are TTL level signals. In previous implementations of the scanner control system, noise was a significant problem in the encoder circuit. When noise causes spurious pulses, errors are caused in the feedback causing position errors that induce sudden unpredictable motion in the motors.

The primary problem with using the encoder TTL level outputs with relatively long cable length is poor nois immunity. This problem becomes compounded when the environment in which the system operates is noisy. The solution to the problem is a secondary output buffer having open-collector outputs that are able to sink a large amount of current. The signals are then pulled up to +5 volts through 150 ohm resistors and sent to Schmitt trigger inputs on the board that uses the signals. A 10-conductor ribbon cable carries the signals from the buffer and regulator circuit to the appropriate encoder board. This cable has interlaced ground conductors to provide further noise immunity.

A secondary source of noise is the long run of cable carrying the +5 volt supply line. This is solved by providing an unregulated +8 volt source to a +5 volt regulator mounted,

along with the buffer circuitry, to the back of the encoder. Hence, the supply is regulated at the encoder and induced noise is minimized. All of the circuitry mentioned is contained within a grounded metal enclosure mounted to the back of each encoder.

4.2.2.2 Circuit Description

The open-collector buffer circuit, shown in figure 4-9, consists of one noninverting hex buffer/driver with open-collector high voltage outputs capable of sinking up to 40 mA. This integrated circuit gets its power from the 7805 +5 volt 1 amp voltage regulator. This regulator also supplies +5 volts to the encoder. The inputs of the buffers are connected to the signal outputs of the optical encoder. The outputs of the buffers are connected to a 10-conductor ribbon cable connector. The pin configuration of the cable connector was designed so that if plugged in upside down no damage will result to the power supply or the encoder. The entire assembly is housed within a small aluminum box that is connected to ground by way of the heat sink tab on the regulator.

4.2.3 Fan-Beam Encoder Card

4.2.3.1 Device Description

The Fan-Beam Encoder Card allows the microprocessor to read the position of the fan-beam degree of freedom. The absolute position of the fan-beam may be determined by counting pulses

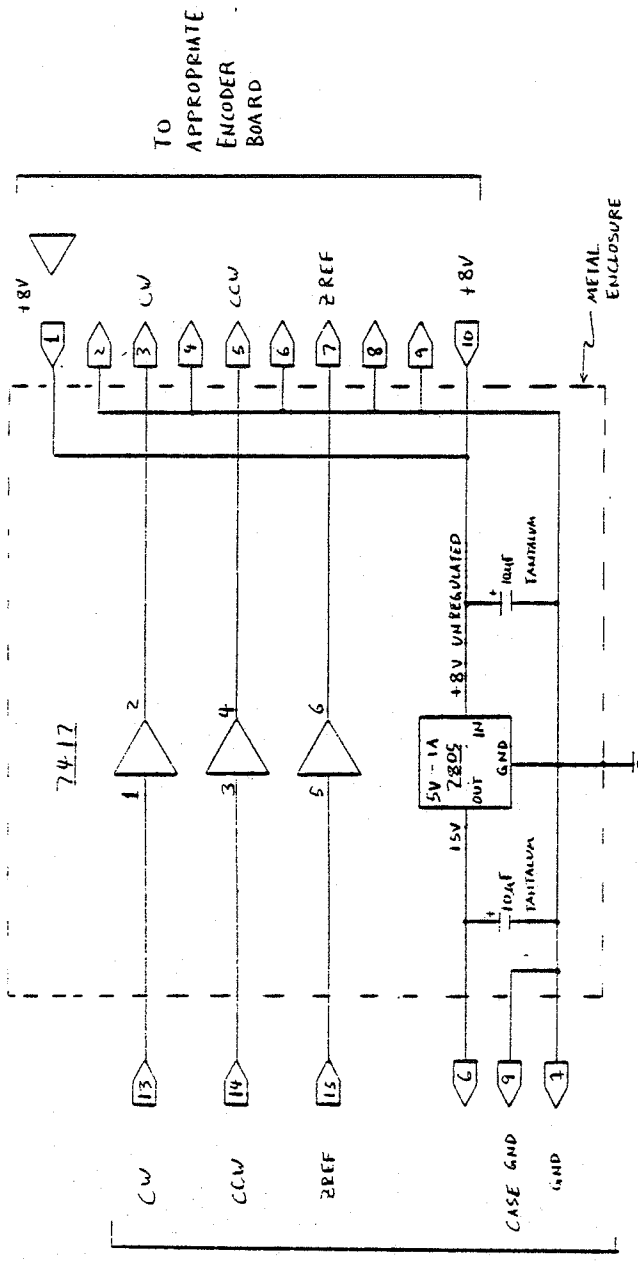


Fig. 4-9 Open-Collector Buffer/Regulator Circuit

from the fan-beam encoder. Since it is planned to incorporate a mechanical advantage of 4 to 1 (encoder to fan-beam rotation), the effective encoder resolution will be increased fourfold to 40 ticks per degree. It was assumed that the fan-beam would pass through a maximum angular displacement of 90 degrees. Since 40 ticks are produced in one degree of fan-beam rotation, a 90 degree angular displacement would produce 3600 ticks, necessitating a 12-bit counter. It is important to realize that the cocking degree of freedom also moves the position of the receiving arm, hence the absolute position of the receiving arm may be determined by adding the cocking angle with the relative fan-beam angle. To maintain a 90 degree scan sweep, the fan-beam encoder may exceed the maximum count allowed by a 12-bit counter and hence lose positional information. A fourth counting stage was added, expanding the counter to 16 bits, to prevent this occurrence. In addition this stage provides sign bit propagation to allow automatic two's complement representation of negative angles.

Since the counters power up in a random state the zero reference line of the encoder is used to reset the counters. At 16-bits of counter magnitude, the encoder can be rotated through an angular displacement of 719.8 degrees, if the zero reference is placed in the middle of the rotation, without overflowing the counter. This is depicted in figure 4-10.

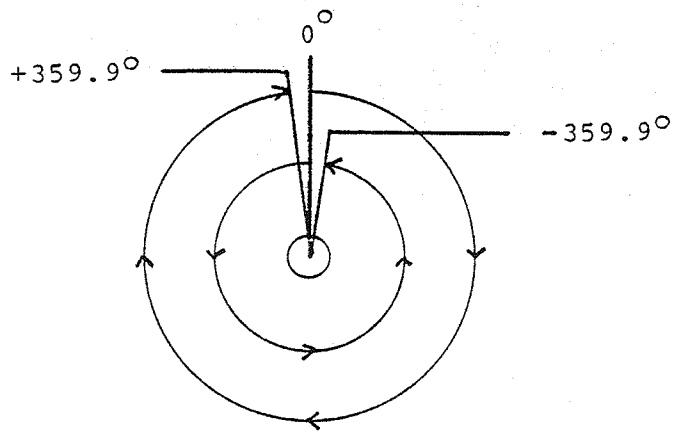


Fig. 4-10 Extents of Rotation of the Fan-Beam Encoder

Given that a fan-beam sweep consists of a 90 degree rotation of the receiver arm (360 degree rotation of the encoder shaft), theoretically the receiver arm may be cocked up to 45 degrees in either direction before the encoder will roll over the zero reference (at +360 or -360) and lose positional information.

The Fan-Beam Encoder Card contains two 8-bit position registers that together specify a 16-bit fan-beam position at which a "take data" interrupt is to be issued to the Interdata. The Interdata should service this interrupt by reading the appropriate data from the Data Aquisition System. A control register is provided to enable or disable the production of these interrupts.

In causing interrupts by hardware, a hybrid software/hardware approach is used. Various resolutions (number of data points taken per degree) may be obtained under software control by varying the incremental values which are repetitively loaded into the position register. In this manner, small sections of tissue may be investigated at higher resolutions using the same reconstruction algorithm.

Incidental logic on the board enables interrupts to be produced from devices external to the control system and provides address decoding for both read and write operations. A line is provided to reset the interrupt request; this line also resets flip-flops that register the passing of the various encoders through their zero reference point.

4.2.3.2 Programming Considerations

The fan-beam position may be read from addresses 7FF8H and 7FF9H. Address 7FF8H contains the low order 8-bits of position information, while 7FF9H contains the high order 8-bits of position information. This conforms to the conventional "LO-HI" 16-bit microprocessor representation.

The positional interrupt control register provides a means of causing hardware driven interrupts that are software controllable. Hence, the SYM-1 is relieved of constantly noting position for the purpose of sending interrupts to the Interdata. The SYM-1 must only realize that an interrupt has

occurred (the position causing data to be taken has been passed) and reload the positional interrupt control register to prepare for the next data point. Two methods are available to the programmer to allow the realization that an Interdata interrupt has been issued. The first approach is implemented by tying the Interdata interrupt line to one of the VIA data available handshake lines; this causes a SYM-1 interrupt. The second approach is to poll an input port which contains the Interdata interrupt line as one of its bits. This port is provided for on the Rotational/Cocking Encoder Board and will be discussed in the section covering that circuit.

When an interrupt occurs, no matter which method is used for detection, the same action should be performed. First, the positional interrupt control registers should be updated with the next point at which data is to be taken, then the Interdata interrupt flip-flop should be reset by performing a write operation to location 7FFEH.

The positional interrupt control register is composed of two 8-bit registers, the first register, located at 7FF8H, holds the low order position, while the high order position is held in the 8-bit register located at 7FF9H. At the start of a scan these registers should be loaded and the positional interrupts enabled (by setting bit-0 of the positional interrupt enable register located at 7FFAH). Upon completion

of the data taking portion of the scan, bit-0 of positional interrupt enable register should be reset to disable further generation of positional interrupts. The Interdata interrupt flip-flop should also be reset by writing to location 7FFEH.

A signal line that allows interrupts to be caused by external devices (EXTINT) is provided for in the controller design. This signal is OR'ed with the output of the Interdata interrupt flip-flop to form the Interdata interrupt line. Because of this arrangement it is important that the programmer both reset the Interdata interrupt flip-flop as well as disable the positional interrupts to avoid conflicts at the OR gate.

A list of memory locations that are serviced by the Fan-Beam Encoder Card, and their respective functions, is provided for reference in figure 4-11.

Address	Operation	
	Write	Read
7FF8H	Positional Interrupt Control Register LO	Fan-Beam Position LO
7FF9H	Positional Interrupt Control Register HI	Fan-Beam Position HI
7FFAH	Positional Interrupt Enable Register Bit 0 = 1 Enable Bit 0 = 0 Disable	
7FFEH	Reset Positional Interrupt Flip-Flop Reset Passed Zero Flip-Flops	

Fig. 4-11 Fan-Beam Encoder Memory Map

4.2.3.3 Mechanical Effects on Resolution

It should be apparent that the gear ratio between the receiver arm shaft and the encoder shaft is of importance when resolution is being considered. Let N1 be the number of rotations of the encoder shaft for N2 rotations of the receiver arm. Then the effective resolution of the encoder is (10 * N2)/N1 ticks per degree. To compute the actual position of the arm, the value within the fan-beam position counter should be multiplied by the factor N1/N2.

It is most appropriate to choose gear ratios as multiples of 2. In this manner, higher resolution may be accomplished with reprogramming involving the shifting of an assumed decimal point by one bit.

4.2.3.4 Circuit Description

The Fan-Beam Encoder Circuit consists of a set of Schmitt triggers to receive pulses from the encoder, a 16-bit up-down counter to count these pulses, two 8-bit registers to hold the position at which an interrupt should be issued, and a set of comparators to determine when the counter value matches the register value. A control register is provided to allow the interrupts to be disabled and additional logic provides address decoding for read and write operations. The circuit diagram of this board may be seen in figure 4-12.

The open-collector buffered encoder outputs are pulled up with 150 ohm resistors to +5 volts and then enter the Schmitt trigger inputs of IC15a, b, c. The inverted $\overline{CW}$ signal is sent to the up-count clock of IC3 while the inverted $\overline{CCW}$ line is tied to the down-count clock of IC3. The zero pulse is output coincident with the $\overline{CW}$ or $\overline{CCW}$ pulse. ZREF is connected through IC15d to clear all of the counters. Since the counter clocks on the rising edge while the the clear line is active high level sensitive, a race condition exists at the falling edge of ZREF. This race condition is eliminated by delaying ZREF through an RC network between the output of IC15c and input of IC15d. The delay allows the clear pulse to remain active through the trailing edge of $\overline{CW}$ or $\overline{CCW}$. The fan-beam position counters IC3, IC4, IC5, and IC6 are all connected in cascade. The outputs of low order position counters IC3 and IC4 are sent to tristate bus driver

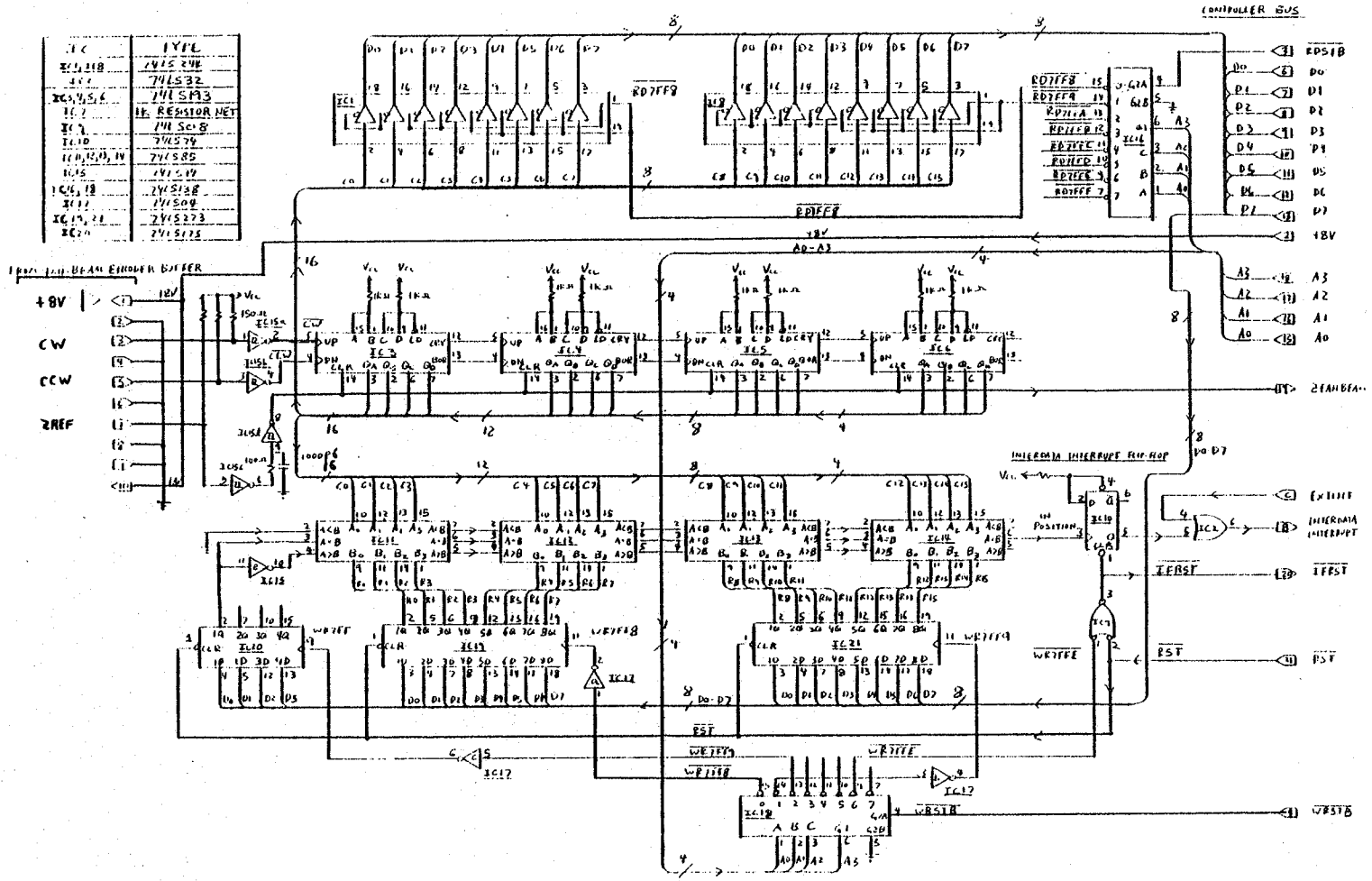


Fig. 4-12 Fan-Beam Encoder Card Circuit Diagram

IC1 while the outputs of the high order position counters IC5 and IC6 are connected to bus driver IC8. The position counter outputs are also sent to the A-inputs of comparators IC11, IC12, IC13, and IC14. These comparators are wired in cascade to detect the condition of A=B where the B-inputs are provided by 8-bit positional interrupt control registers IC19 (low order) and IC21 (high order). When a match occurs, A=B goes high and clocks a logical 1 into the Interdata interrupt flip-flop IC10. This causes an interrupt through OR gate IC2. The OR gate is provided to allow other external devices to cause Interdata interrupts by way of bus pin C - EXTINT. As mentioned in the previous section on programming, it is the responsibility of the microprocessor program to disable the positional interrupts and reset flip-flop IC10 by writing into location 7FFEH. This prevents a conflict at the OR gate and allows the EXTINT line to be used as described.

The lowest order bit of 4-bit register IC4 is used to enable and disable the interrupts by way of the cascade inputs of low order comparator IC11. The remaining three bits remain unused and are available for future applications. One-of-eight decoder IC16 provides read address decoding and strobes for enabling the tristate bus drivers. If address line A3 is high, address lines A0 through A2 select which output line should be asserted low when $\overline{\text{RDSTB}}$ is brought low. The output lines of the decoder enable bus driver IC1 to send the value of low order counters IC3 and IC4 out to the bus if

address lines read 7FF8H. The high order counter (IC5 ,IC6) outputs are sent out to the bus by bus driver IC8 when the address lines read 7FF9H and a $\overline{\text{RDSTB}}$ signal is present.

One-of-eight decoder IC18 provides write address decoding and strobes for the positional interrupt control registers IC19 and IC21, as well as interrupt enable register IC20. If address line A3 is high, address lines A0 through A2 select which output should be asserted low if $\overline{\text{WRSTB}}$ is brought low. Since the registers latch on the rising edge, these output lines are inverted by IC17a, IC17b, and IC17c to provide positive going latch strobes to IC19, IC21, and IC20, respectively. The low order positional interrupt control register IC19 latches the data bus if address 7FF8H is written to, while high order register IC21 latches the data bus if address 7FF9H is written to. The positional interrupt enable register IC20 latches the low order 4 bits of the data bus if address 7FFAH is written to. A write operation to address 7FFEH causes the Interdata interrupt flip-flop IC10 to be reset and pulses the $\overline{\text{IFRST}}$ line low to reset the passed-zero flip-flops on the Rotational/Cocking Encoder Card.

A system reset will clear the positional interrupt control registers (IC19, IC20), clear (disable) the positional interrupt enable register IC20, clear the Interdata interrupt flip-flop IC10, and reset the passed-zero flip-flops by

pulsing $\overline{\text{IFRST}}$ low through IC2a.

4.2.4 Rotational/Cocking Encoder Circuit

4.2.4.1 Device Description

The Rotational/Cocking Encoder Circuit permits the microprocessor to read the position of both the rotational and cocking degrees of freedom. These positions are determined by counting pulses from the respective optical encoders. The optical encoders used have a resolution of 10 ticks per degree or 3600 ticks per revolution. Two 12-bit counters are used to count these pulses, one for each degree of freedom, allowing an encoder shaft rotation of +204.7 degrees through -204.8 degrees without loss of positional information due to counter overflow. This specification assumes that the zero reference is placed in the middle of the angular deflection as shown in figure 4-13.

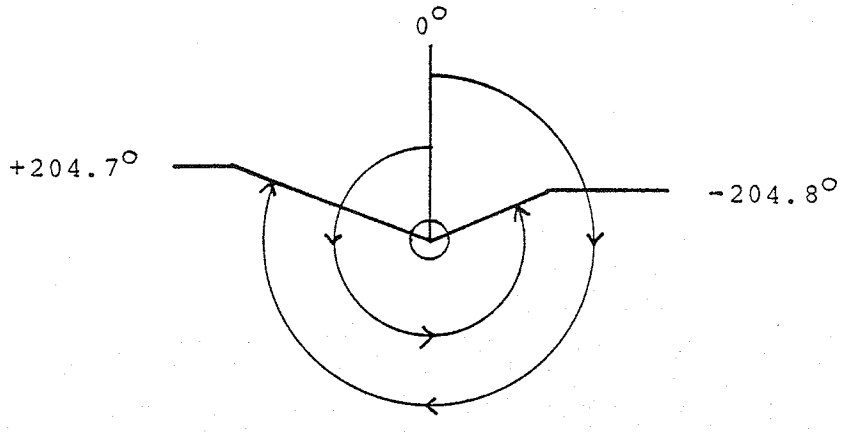


Fig. 4-13 Extent of Encoder Shaft Rotation for Cocking and Rotational Degrees of Freedom

The full extent of these encoders is not used, primarily because the linkage between the degrees of freedom and their respective encoders is one-to-one but also because these degrees of freedom never rotate through angles more than 360 degrees. In most cases the degrees of freedom will rotate through angles significantly less than 360 degrees.

In addition to the counters and related circuitry to receive the encoder outputs, decode addresses, and send information to the bus, flip-flops are provided to latch the crossings of the encoders through the zero reference point.

4.2.4.2 Programming Considerations

The position of the cocking degree of freedom may be read from address 7FFAH and 7FFBH. Address 7FFAH contains the low order 8-bits of position information, while address 7FFBH contains the high order bits of position information. The position of the rotational degree of freedom may be read from address 7FFCH and 7FFDH. Address 7FFCH contains the low order 8-bits of position data and address 7FFDH contains the high order bits of positional data.

Since the position counters power up in a random state, the zero reference lines of the encoders are used to reset the counters. It is important to know that each encoder has passed through its zero reference point as this certifies that the values of the counters are in fact the actual

position of the degree of freedom in question. A flip-flop latches the zero reference signal from each encoder. The states of these flip-flops may be read from location 7FFEH. Refer to the memory map in figure 4-14 for the bits of 7FFEH and their meanings.

Address	Read Operation
7FFAH	Cocking Position Low
7FFBH	Cocking Position High
7FFCH	Rotational Position Low
7FFDH	Rotational Position High
7FFEH	Passed-Zero Flag/ Interdata Interrupt
	Bit 0 - Fan-Beam passed zero
	Bit 1 - Cocking passed zero
	Bit 2 - Base Rotation passed zero
	Bit 3 - Interdata interrupt
	Bit 4-7 - Unused

Fig. 4-14 Rotational/Cocking Encoder Circuit Memory Map

When a degree of freedom passes through zero its respective bit goes high. Bit-3 is used to observe the state of the Interdata interrupt line. This would be used if one were polling to determine when the Interdata had been interrupted. Refer to the programming considerations of the Fan-Beam Encoder Card for more information concerning determination of the state of this interrupt line. When a system reset occurs, or memory location 7FFEH is written into, all four of the status bits are cleared.

It is suggested that upon power up, the software should

initialize all three degrees of freedom by rotating each degree of freedom from limit to limit until each respective passed-zero bit goes high. The cocking degree of freedom should seek zero first, then the fan-beam, and finally the base rotation. Limit status information is available from the limit status byte provided by the External Event Card at address 7FF0H.

4.2.4.3 Mechanical Effects on Resolution

Though the encoder shaft is mounted directly to the rotational degree of freedom (the gear ratio is 1:1), at some point it may be desired to increase this ratio by some factor. The cocking degree of freedom possesses an encoder shaft to degree of freedom gear ratio of close to 9.5 to 1. Let N1 be the number of rotations of the encoder shaft for N2 rotations of the degree of freedom in question. The effective resolution of each encoder then becomes (N2 * 10)/N1 ticks per degree. It is important that the exact cocking angle be known, as this value must be added to the relative fan-beam position to determine the absolute fan-beam position. Care should be taken to find exact gear ratios in the present system and choose new gear ratios for future implementations to ease the conversion between the observed encoder angle and actual physical angle. To compute the physical angle from the observed encoder angle the encoder angle should be multiplied by the correction factor N1/N2.

When choosing ratios it is most appropriate to choose gear ratios as multiples of 2. In this manner, higher resolution may be attained with the only reprogramming implication being that of shifting an assumed decimal point by one bit.

4.2.4.4 Circuit Description

The Rotational/Cocking Encoder Card consists of two sets of Schmitt triggers to receive pulses from the encoders, two sets of 12-bit up-down counters to count the pulses, and two sets of tristate bus drivers to allow the counter values to be presented to the controller data bus. In addition, address decoding is provided for the enabling of the bus drivers, three flip-flops store the zero reference crossing event on all the degrees of freedom, and a bus driver is present to send the states of the flip-flops out to the controller data bus. A circuit diagram of the Rotational/Cocking Encoder Card can be found in figure 4-15.

The open-collector buffered encoder outputs are pulled up with 150 ohm resistors to +5 volts before entering the Schmitt trigger inputs of IC7a, IC7b, IC7c and IC7d, IC7e, IC7f. The inverted $\overline{CW}$ signal, at IC7d, from the cocking encoder is sent to the up-count clock input of IC2 while the inverted $\overline{CCW}$ signal at IC7e is sent to the down-count clock input of IC2. The rotational encoder is mounted back-to-back with the shaft of the rotational degree of freedom. Therefore, a clockwise motion of the degree of freedom will

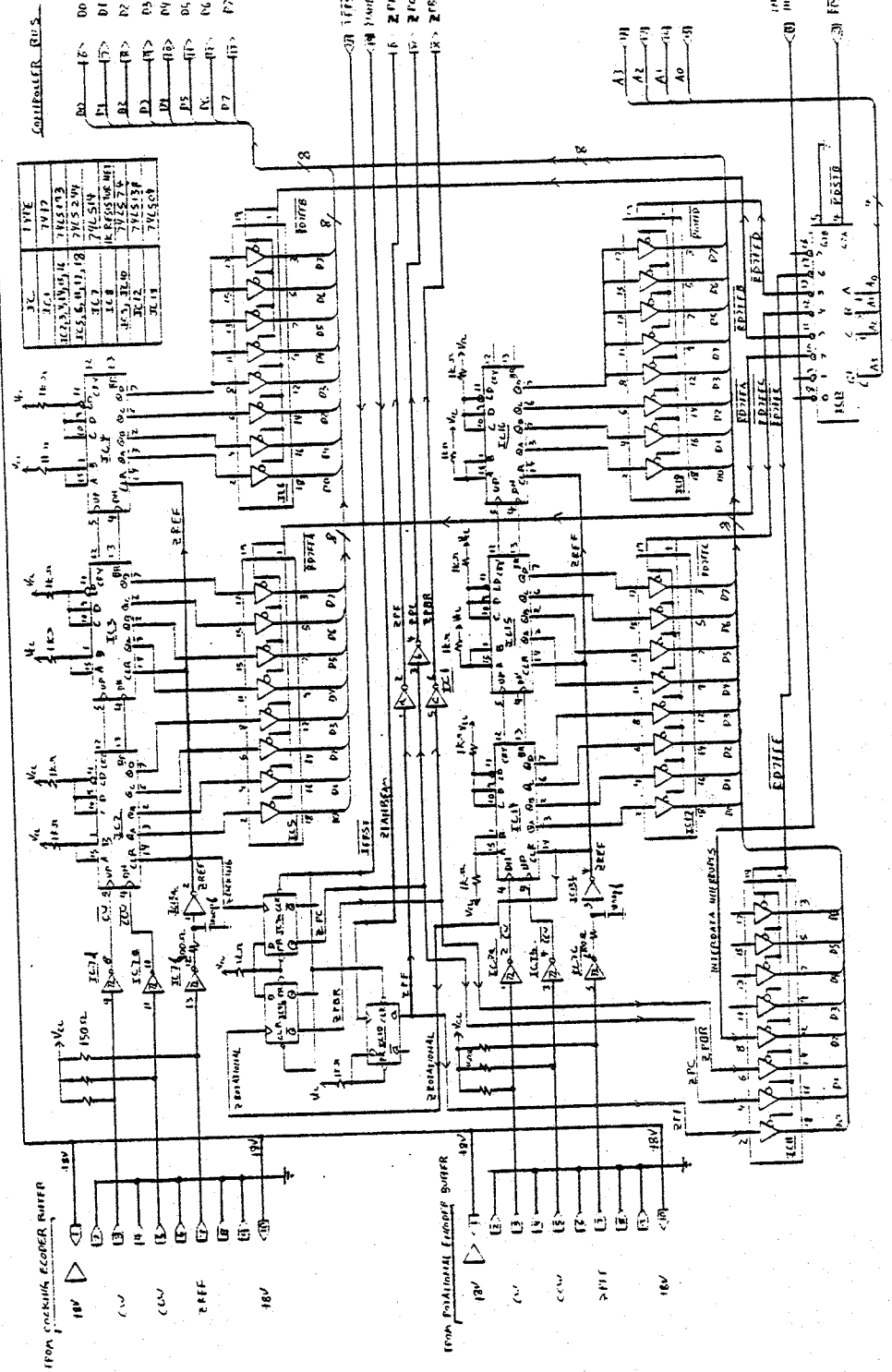


Fig. 4-15 Rotational/Cocking Encoder Card Circuit Diagram

produce a counterclockwise motion in the encoder. To correct for this the inverted $\overline{CCW}$ signal of the rotational encoder, at IC7b is sent to the up-count clock input of IC14, while the inverted $\overline{CW}$ signal at IC7a is sent to the down-count clock input of IC14. The zero pulse is output on ZREF coincident with the $\overline{CW}$ or $\overline{CCW}$ pulse. The ZREF lines of both encoders are connected through IC13a, IC13b to clear their respective counters IC2, IC3, IC4 and IC14, IC15, IC16. Since the counters clock on the rising edge while the clear input is active high level sensitive, a race condition exists at the falling edge of ZREF. This race condition is eliminated by delaying ZREF of each encoder through an RC network between the output of IC7f, IC7c and the input of IC13a, IC13b. This delay allows the clear pulse to remain active through the trailing edge of CW or CCW. The counters IC2, IC3, IC4 and IC14, IC15, IC16 are connected in cascade to form two 12-bit counters. The outputs of low order position counters IC2, IC3, and IC14, IC15 are sent to tristate bus drivers IC5 and IC17, respectively. The outputs of the high order position counters IC4 and IC16 are sent to bus drivers IC6 and IC18. The high order 4-bits of drivers IC6 and IC18 are tied to the most significant bit of the position counters. This provides propagation of the sign, assuming that angles of +204.7 or -204.8 are not exceeded. Propagation of the sign bit is useful when performing

mathematical operations as it preserves two's complement representation.

One-of-eight decoder IC12 provides read address decoding and strobes for enabling the tristate bus drivers. If address line A3 is high, address lines A0 through A2 select which output line should be asserted low if $\overline{\text{RDSTB}}$ is brought low. Drivers IC5, IC6, IC17, IC18, or IC11 are enabled to send their input data to the data bus if addresses 7FFAH, 7FFBH, 7FFCH, 7FFDH, or 7FFEH are read from.

D-type flip-flops IC9 and IC10 have their D inputs tied high and their clock inputs connected to the encoder ZREF lines of the three degrees of freedom. On the rising edge of ZREF a logic 1 is clocked into the appropriate flip-flop. Base rotation ZREF is fed to the clock input of IC9b, cocking ZREF is fed to the clock input of IC9a, and fan-beam ZREF is fed over the bus to the clock input of IC10a. All flip-flops have their clear line tied to IFRST which is sent from the Fan-Beam Encoder Card. This signal resets the flip-flops on system reset or if address 7FFEH is written to. The outputs of IC10a, IC9a and IC9b are fed to input bits 0, 1, and 2, of bus driver IC11. In addition, these outputs pass through open-collector driver IC1 and go over the bus to illuminate the passed-zero LED's on the Manual Control Pod.

Input bit-4 of tristate bus driver IC11 is tied to the Interdata interrupt line. This allows the state of this line to be determined by reading location 7FFEH. The remaining high order 4-bits of IC11 are unused and are available for future applications.

4.2.5 Mechanical Calibration and Alignment

Both Rotational/Cocking and Fan-Beam Encoder Boards assume that the encoders of their respective degrees of freedom are aligned such that the zero reference pulse ZREF occurs in the exact middle of the allowed angular displacement for that degree of freedom. The scanner may be calibrated by moving gears or couplings that are attatched to the encoders by loosening their set screws and rotating the encoder shaft to the appropriate position. The zero reference LED's provide a means of detecting when the encoder has passed through zero. Refer to the device descriptions of the Rotational/Cocking and Fan-Beam Encoder Board sections to determine appropriate encoder alignment. Fine positioning of the fan-beam may be accomplished by rotating the receiver arm by hand, independent of shaft motion. Fine positioning of the cocking degree of freedom may be accomplished by rotation of the transmitter about the transmitter shaft.

4.3 External Event Detection and Limit Controls

4.3.1 External Event Card

4.3.1.1 Device Description

During the operation of the scanner, the microprocessor must be able to detect that a limit condition exists on one of the degrees of freedom. This limit status information must also be made available to the PWM boards via the controller bus. An emergency stop signal, when detected, must limit the

motion of all degrees of freedom in both directions. A system reset is the only method available to reset the emergency stop state once entered. Finally, a switch is provided to allow selection between manual and automatic modes of operation and a flashing LED indicates that manual mode is active. Both the switch and the LED are mounted on the Manual Control Pod.

Limit conditions are detected by opto-interrupters. In normal non-limiting conditions, the beam between the LED and phototransistor is not broken, allowing the phototransistor to conduct. When the path is broken by the degree of freedom moving into a limiting position, the phototransistor no longer conducts. This is detected by the External Event Board and made available to the microprocessor.

The External Event Board contains one read port that may be DIP-switch addressed anywhere with in the address space from 7FF0H to 7FFFH. The 16 possible switch positions and their respective addresses are outlined in figure 4-16.

Read Address	Switch Setting S4	S3	S2	S1
7FF0H	C	C	C	C
7FF1H	C	C	C	O
7FF2H	C	C	O	C
7FF3H	C	C	O	O
7FF4H	C	O	C	C
7FF5H	C	O	C	O
7FF6H	C	O	O	C
7FF7H	C	O	O	O
7FF8H	O	C	C	C
7FF9H	O	C	C	O
7FFAH	O	C	O	C
7FFBH	O	C	O	O
7FFCH	O	O	C	C
7FFDH	O	O	C	O
7FFEH	O	O	O	C
7FFFH	O	O	O	O

NOTE: O = Switch open (OFF), C = Switch closed (ON)

Fig. 4-16 External Event Address Selector Settings

Care should be taken so as not to have two boards read addresses to the same location. If this situation occurs, a bus conflict will result and the information read will be invalid. For the implementation of this control system, the External Event Board limit status port is addressed to 7FF0H.

4.3.1.2 Programming Considerations

The limit status port, addressed at 7FF0H allows the programmer to determine the limit status of any degree of freedom in any direction. The meaning of each bit is dependent upon how the limit controls are implemented. A description of the limit status bits and their meanings is presented in figure 4-17.

Bit Position	Function
0	Rotational Clockwise Limit
1	Rotational Counterclockwise Limit
2	Cocking Clockwise Limit
3	Cocking Counterclockwise Limit
4	Fan-Beam Clockwise Limit
5	Fan-Beam Counterclockwise Limit
6	Unused - For Future Expansion
7	Unused - For Future Expansion

Fig. 4-17 Bit Map of the Limit Status Port

These bits are normally zero in the non-limited state. When a limit condition arises, the bit associated with that limit condition goes high. If the emergency stop switch has been depressed, all of the bits go high (all degrees of freedom are limited in both directions). As mentioned previously, the emergency stop condition can only be cancelled by a full system reset.

4.3.1.3 Circuit Description

The External Event Detection and Limit Control Card consists of a tristate bus driver to output limit status information to the control bus, related address decoding for this driver, and a flip-flop that is set when the emergency stop switch is depressed. Related logic to hold all limit bits high, when the emergency stop line is active, is also present on the board. A manual/automatic mode select switch provides input to the control bus as to the mode of operation, and enables

an NE555 to run in astable mode and flash an LED indicating that the system is in manual mode. A 40-conductor connector is provided to allow external signals to enter the board. Interlaced ground lines within this cable increase the noise immunity. A circuit diagram of this board may be found in figure 4-18.

Each opto-interrupter is provided with an LED current source and ground, as well as a phototransistor signal line and ground. The opto-interrupters specified (GE H13B1) have photo-darlington outputs capable of sinking 2.5 mA. Pull-up resistors having a value of 4K are connected between the phototransistor collector and +5 volt supply, while the phototransistor emitter is connected to ground. The collectors are also connected to one input of OR gates IC8 and IC9. When a limiting condition exists, the light beam is broken in the interrupter and the phototransistor no longer grounds the OR gate input, this input is then pulled high by the 4K resistor. The second input to the OR gates are all tied together to the output of the emergency stop flip-flop IC5. When this output goes high it forces all OR gate outputs high, thereby limiting all degrees of freedom. The OR gate outputs go on to the PWM board via the controller bus; these outputs also pass on to tristate bus driver IC7.

Bus driver IC7 is enabled to send the data present at its inputs out to the control bus by way of NAND gate IC3a if

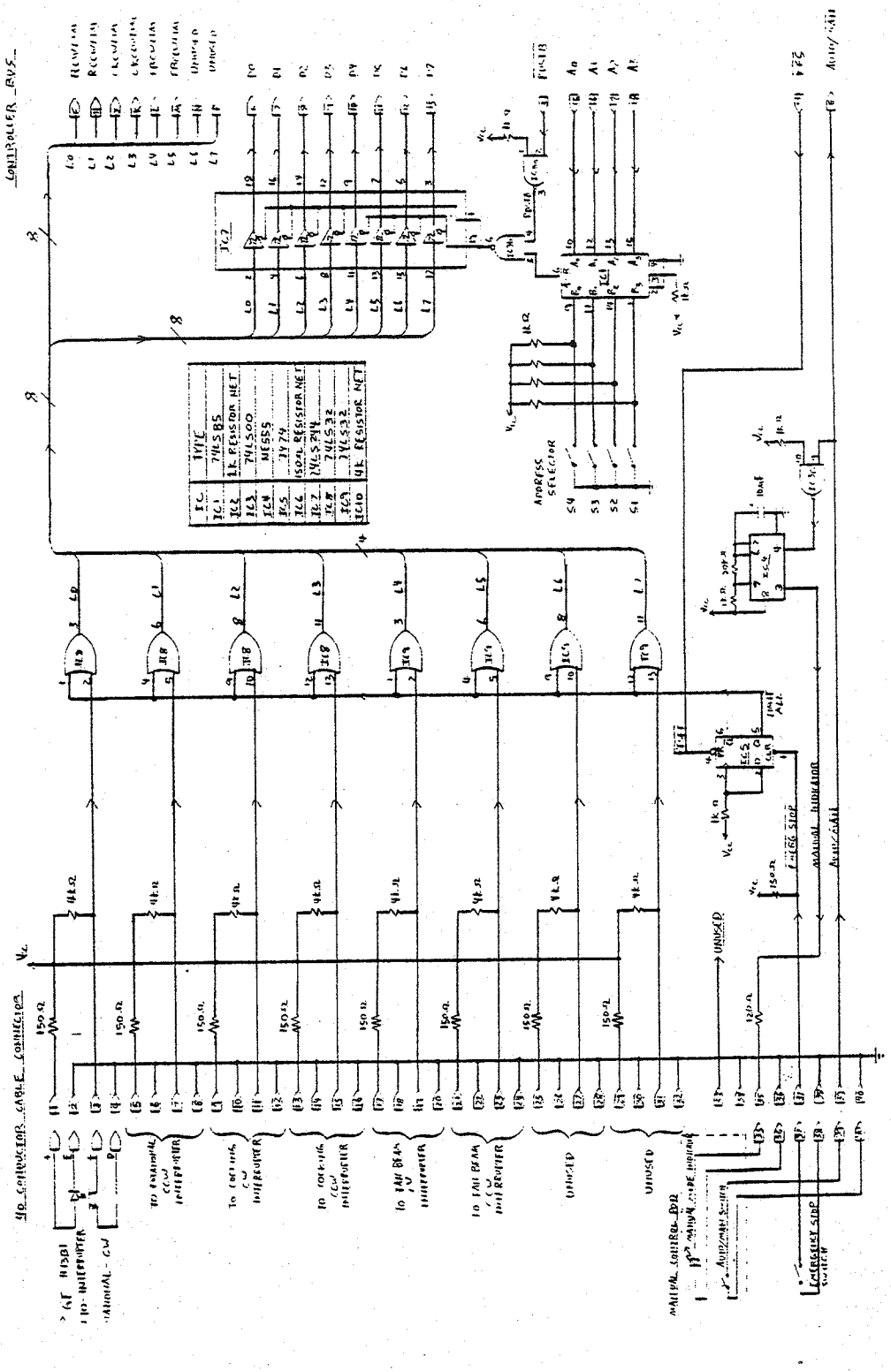


Fig. 4-18 External Event Card Circuit Diagram

$\overline{\text{RDSTB}}$ is low and an address match exists (IC1 compares the address bus with the DIP-switch address settings).

The automatic/manual mode select switch forwards its signal on to controller bus pin E. NAND gate IC3a acts as an inverter to provide an enable signal to pin 4 of IC4. IC4 is an NE555 timer operating in astable mode. This provides a pulsating current source to an indicator LED when manual control is operative. A 120 ohm current limiting resistor is provided to protect the LED. Both the auto/manual mode select switch and the LED are located on the Manual Control Pod.

4.4 Manual Control Interface

4.4.1 Manual Control Card

4.4.1.1 Device Description

The purpose of manual control is to provide the operator with a means of controlling each degree of freedom independent of the SYM. This is important for setting up the scanner alignment and taking stationary readings as well as manually initializing the encoder counters.

Each manual control card contains circuitry for controlling two PWM Cards (two degrees of freedom). The PWM Cards to be controlled may be selected by setting addresses on the

8-position DIP-switch located at position Y-D on the manual control vector card. The switch settings and corresponding PWM addresses are presented in figure 4-19.

PWM Address	Switch Pos	Motor 0 S1	S2	S3	Motor 1 S5	S6	S7
7FF0H		O	O	O	O	O	O
7FF2H		O	O	C	O	O	C
7FF4H		O	C	O	O	C	O
7FF6H		O	C	C	O	C	C
7FF8H		C	O	O	C	O	O
7FFAH		C	O	C	C	O	C
7FFCH		C	C	O	C	C	O
7FFEH		C	C	C	C	C	C

NOTE: O = Switch open (OFF), C = Switch closed (ON)

Fig. 4-19 Manual Control Motor Address Switch Settings

The timing generation for manual control is accomplished by counters IC3, IC4, AND gate IC8b, and one-shot IC1. A circuit diagram appears in figure 4-20. There are four states for each manual control board cycle. These states are: enable motor-address-0/send speed byte, enable motor-address-0/send direction bits, enable motor-address-1/send speed byte, and enable motor-address-1/send direction bits. This cycle is produced by the DIR/$\overline{\text{SPEED}}$ line from IC3 and the $\overline{\text{EN0}}$/EN1 line from IC4. In addition, one of the manual control boards is selected by the address provided from the S0 and S1 lines from IC4. Within each state a write strobe pulse is produced by IC8d,

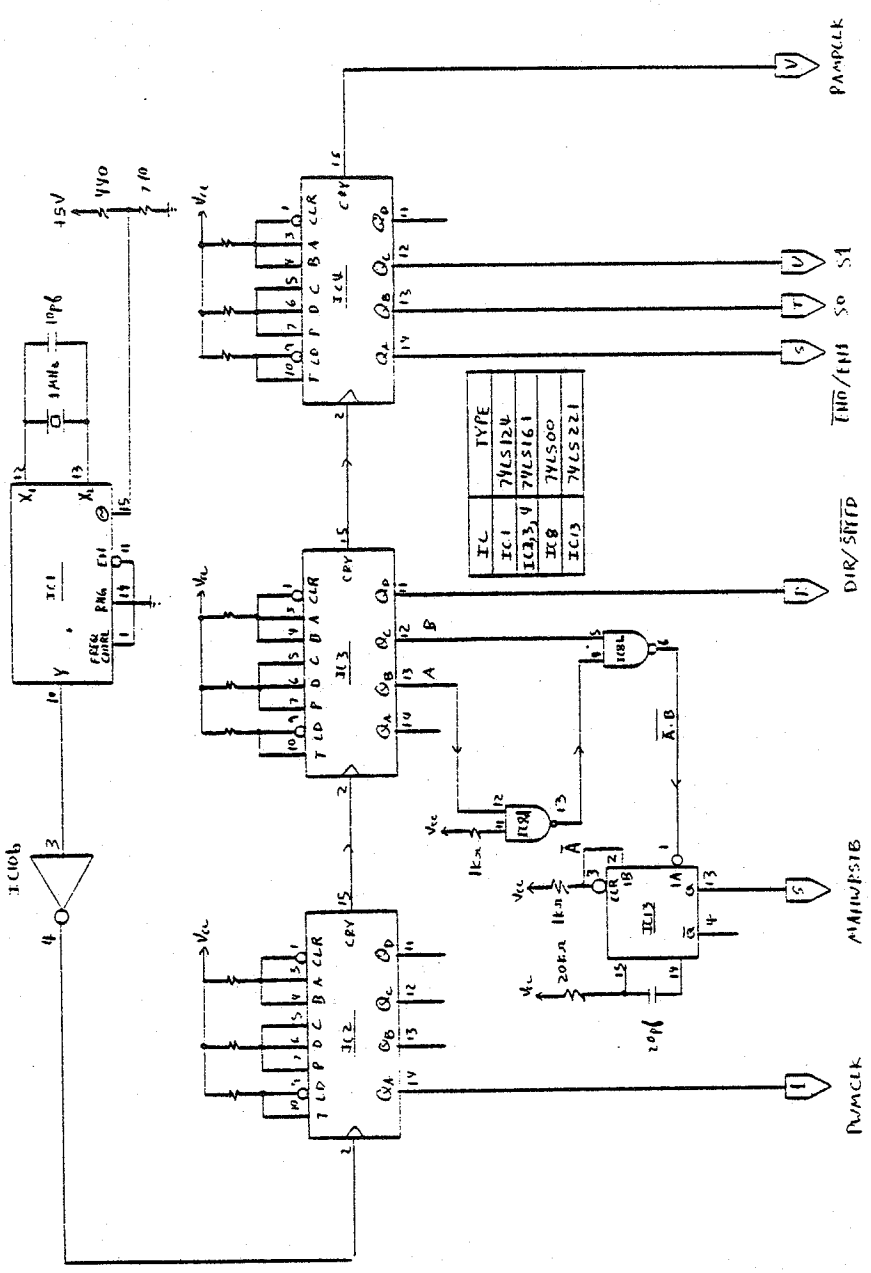


Fig. 4-20 Timing and State Generating Circuitry

IC8b, and one-shot IC1. The one-shot provides a 28 microsecond pulse to write speed or direction data, presented to the contoller data bus by the manual control bus drivers, into the address provided by the manual control address bus drivers. A 244 Hz signal, generated from the carry output of the last counter stage IC4, serves as a clock that is used to drive the velocity ramp generators. A timing diagram of these signals is provided in figure 4-21.

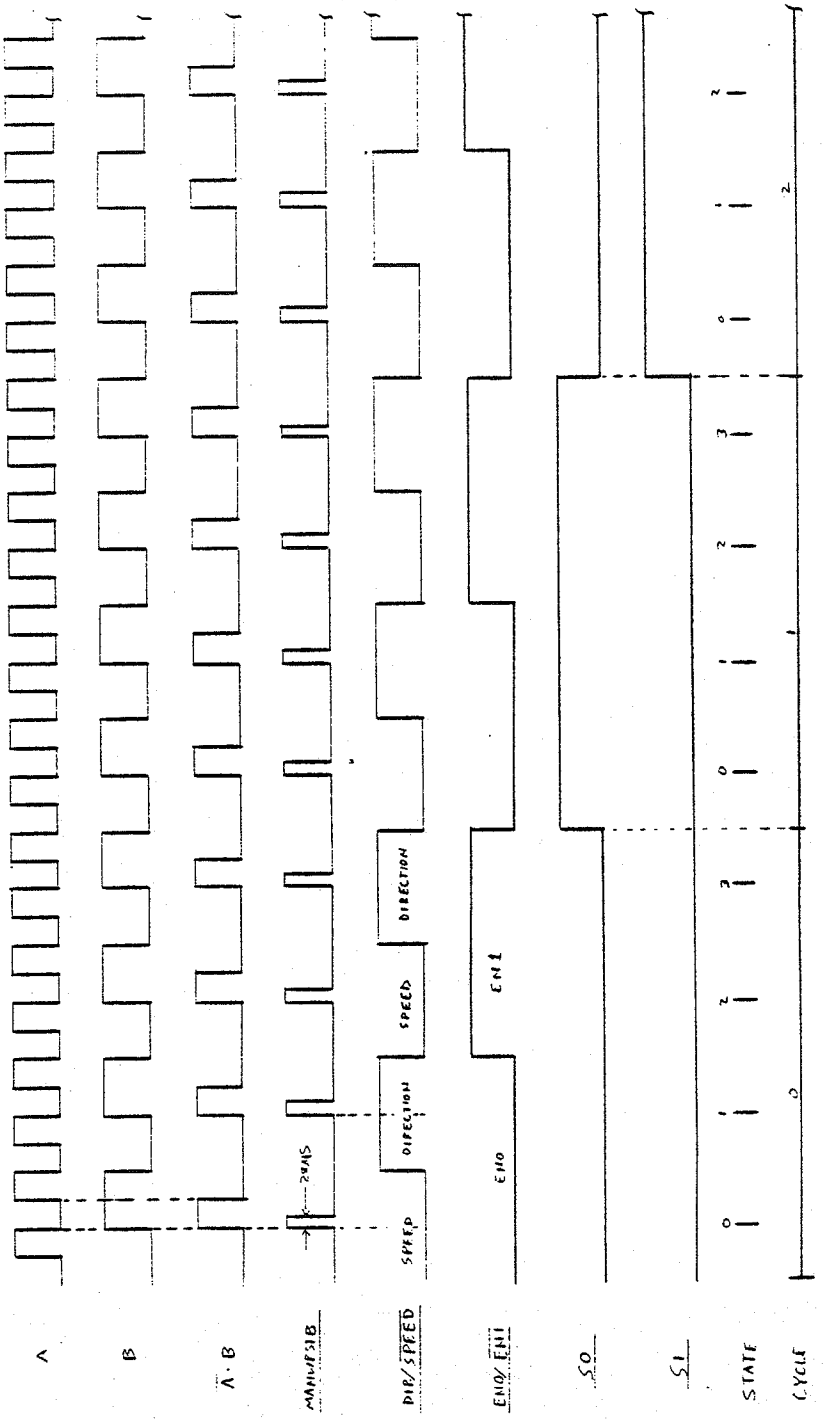


Fig. 4-21 Timing Diagram for Manual Control Timing Signals

The manual conrol circuit will now be discussed; a logic diagram of this circuitry is provided in figure 4-22. The DIR/$\overline{\text{SPEED}}$ line and $\overline{\text{ENO}}$/EN1 line may be thought of as a 2-bit counter, each counter state defining a state of the manual control circuitry. These states are decoded by the one-of-four decoder IC9a. S0 and S1 may also be thought of as a two bit counter, however one state of this counter lasts through all four states of the previous mentioned signals (one cycle of the manual control circuitry). IC9b decodes S0 and S1 and provides an enable-board signal through the board address select DIP-switches SW2.

When manual mode is selected, the tristate bus drivers on the Control System Interface Card are held in the high impedance state; the bus floats and the Manual Control Card, if enabled, may take control of the bus. The $\overline{\text{MAN}}$/AUTO line, connected directly to the mode select switch on the Manual Control Pod, enables the one-of-four decoder IC9b to begin decoding the board-enable states. When the board becomes enabled ($\overline{\text{ENBRD}}$ goes low), IC9a is permitted to decode the four states necessary to complete the cycle. In addition, bus driver IC17b is removed from its high impedance state to allow the manual control write strobe (MANWRSTB) to pass on to the controller bus write strobe line ($\overline{\text{WRSTB}}$). The inverted MANWRSTB then becomes the system WRSTB as the Control System Interface has disabled all of its bus drivers.

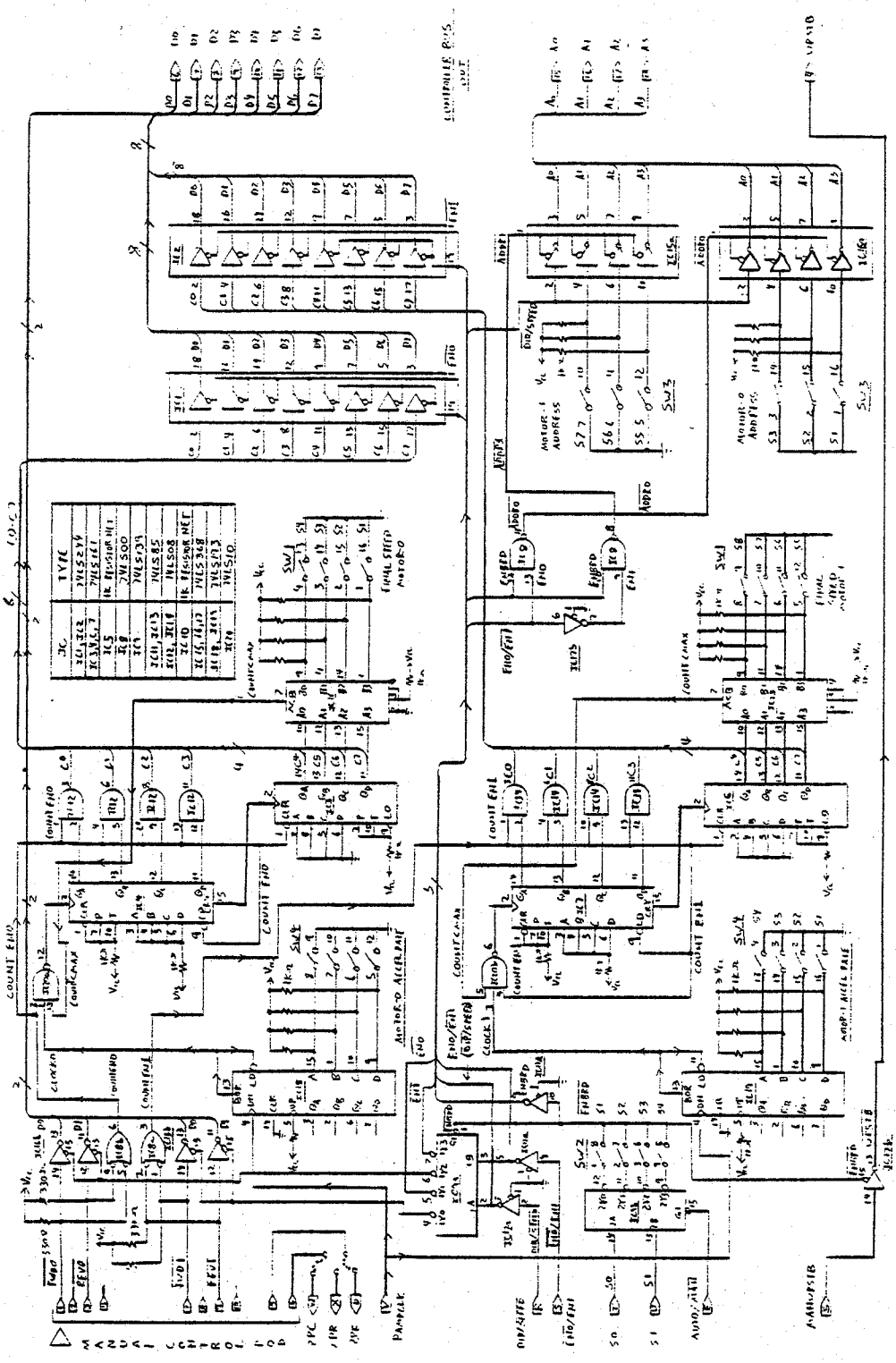


Fig. 4-22 Manual Control Circuit Diagram

The $\overline{EN0}$/EN1 signal enables motor-1 address line bus drivers IC15a when low and motor-0 address bus drivers when high. The three high order address bits are provided by the DIP-switch settings of SW3 while the lowest order bit is tied to DIR/$\overline{SPEED}$. Since these bus drivers invert the data present at the inputs, A0 becomes DIR/$\overline{SPEED}$. This is consistent with the address decoding on the PWM Card. A0 = 0 for writing to the speed control register and A0 = 1 for writing to the direction control register. The DIR/$\overline{SPEED}$ line and $\overline{EN0}$/EN1 line both enter state decoder IC9a. A listing of the states and actions taken during those states is provided in figure 4-23.

State	$\overline{EN0}$/EN1	DIR/$\overline{SPEED}$	Action Taken
0	0	0	Enable motor-1 direction data bus driver IC15b to send direction information over data bus. Enable address bus driver IC15a to send address-1 over address bus. A0 = 1 for direction information.
1	0	1	Enable motor-1 speed data bus driver IC2 to send speed information over data bus. Enable address bus driver IC15a to send address-1 over address bus. A0 = 0 for speed information.
2	1	0	Enable motor-0 direction data bus driver IC16b to send direction information over data bus. Enable address bus driver IC16a to send address-0 over address bus. A0 = 1 for direction information.
3	1	1	Enable motor-0 speed data bus driver IC1 to send speed information over data bus. Enable address bus driver IC16a to send address-0 over address bus. A0 = 0 for speed information.

Fig. 4-23 Functional State Description

Direction information is made available to the direction bus

drivers IC15b, IC16b via the two sets of pushbutton switches. These switches ground the input to the bus drivers when depressed; normally these inputs are pulled high by 330 ohm pull-up resistors. Forward and reverse lines of motor-0 and motor-1 pass through NAND gates IC8b and IC8a, respectively. The outputs of these gates, normally low, enable the ramp generators when brought high by depression of either forward or reverse switches.

The velocity ramp generators consist of counters IC4, IC3 and IC6, IC5 clocked by NAND gates IC20a and IC20b, magnitude comparators IC11, IC13, and AND gates IC12, IC14. The value at the counter outputs increases linearly with time. It is this value that is sent to the PWM card as the speed byte. Hence, the velocity of the motor connected to that PWM will be increased by the increasing speed byte.

The counters IC4, IC3 and IC6, IC5 are disabled from counting by IC20a and IC20b until one of the manual control pushbuttons is depressed. If this occurs, IC8b and/or IC8a enables the counters via count enable lines COUNT EN0 and COUNT EN1. These count enable lines are also connected to the load input of IC4, IC6, the clear input of IC3, IC5 and the inputs of AND gates IC12, IC14. Since the load input lines of counter IC4, IC6 are held high, these counters are loaded with all ones when the count enable line is low. AND gates IC12, IC14 are provided to force the outputs of these

counters, as seen by the speed data bus driver, to zero until a manual control switch is depressed. When a manual control switch is depressed, the AND gates allow the counter outputs to pass through unchanged. Hence the speed byte begins counting up from the value 0FH. The high order 4-bits are 0 because COUNT EN0 and COUNT EN1 are tied to the clear inputs of high order counters IC3 and IC5. The ramp clock frequency is divided by divide-by-n counters IC19 and IC18 and is allowed to pass through IC20b and IC20a as long as COUNT EN0 and COUNT EN1 remain high and the value of the high order counters IC3 and IC4 is less than the preset final speed. Magnitude comparators IC11 and IC13 receive the value of counters IC3 and IC5 as one input while the final speed DIP-switch setting serves as their other input. When the count equals the DIP-switch value, the COUNT<MAX line goes low and prevents the ramp clock pulses from passing through IC20a or IC20b.

The ramp clock is a 244 Hz signal that is divided by IC19 and IC18. These counters are presettable up-down counters operated in the down-count mode. When the borrow output goes low (the counter has reached zero), the counters are reloaded with the values set on the DIP-switch SW4. The borrow output is therefore a divide-by-n output of the down count input, n being set by the acceleration rate DIP-switch. This allows 15 different acceleration rates to be selected.

The manual control switches are connected through a 10-conductor ribbon cable which leads from each manual control board to the Manual Control Pod. Interlaced ground lines are provided with the exception of conductors 5 and 6. These lines are pulled-up to 5 volts through 150 ohm resistors and are provided to the Manual Control Pod to illuminate the passed-zero LED's. By connecting these lines to bus pins W, X, or D, the LED may indicate the passing through zero (initialization) of the position encoder on the cocking, rotational, and fan-beam degrees of freedom. When the degree of freedom in question passes zero, W, X, or D, normally pulled to ground by the open-collector driver on the Rotational/Cocking Encoder Card, is released from ground. This allows current to flow through the LED thereby indicating that the zero point has been passed. When the operator is manually initializing the scanner, this feature provides the needed feedback to determine the initialization status of each encoder.

4.4.1.3 Manual Control Pod Description

The Manual Control Pod provides four sets of CW, CCW switches for the control of the three, and an optional fourth degree of freedom. LED's located between each CW and CCW switch indicate when that degree of freedom has passed through the zero reference point. A manual/automatic mode selector switch is provided to switch between the two modes of

operation. Entering manual mode causes an indicator LED to flash on the pod, indicating that the controls are active.

A circuit diagram of the Manual Control Pod appears in figure 4-24. SW1, SW2, SW3, and SW4 as well as LED1 and LED2 are serviced by the Manual Control Board that controls the fan-beam and cocking degrees of freedom. SW5, SW6, SW7, SW8 and LED3 are serviced by the board that controls the rotational and optional fourth degree of freedom. Auto/Manual selector switch SW9 and manual mode indicator LED4 are serviced by the External Event Board.

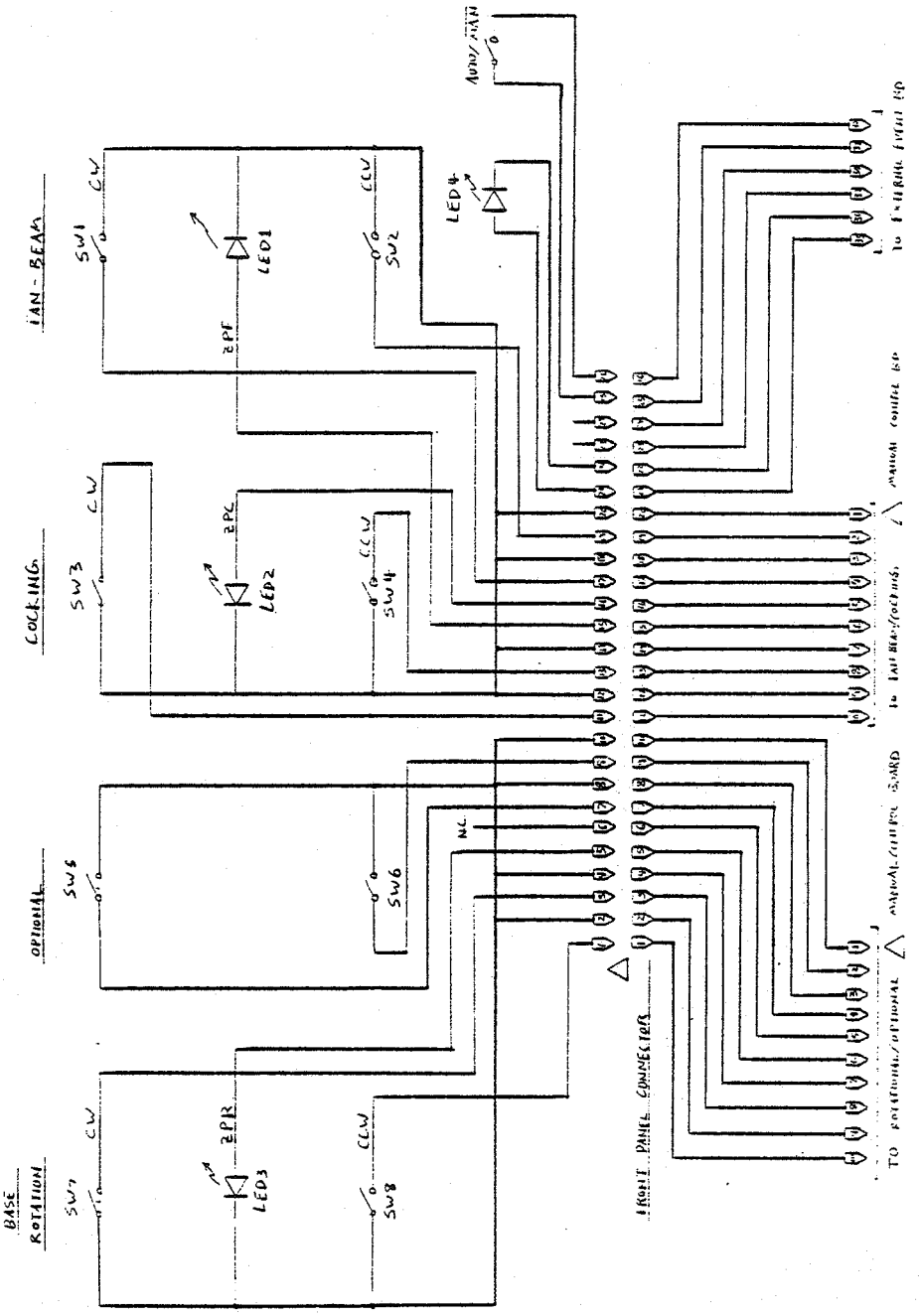


Fig. 4-24 Manual Control Pod Circuit Diagram

Chapter 5

Suggestions for Improvement

5.1 Mechanical Improvements to the Scanner

The present scanner design incorporates gears to achieve motion of the cocking and fan-beam degree of freedom. The position encoders that service these degrees of freedom are also coupled by gears. In an effort to eliminate backlash, and thereby increase the positional accuracy of the data acquisition interrupts, it is suggested that these gears be replaced by a timing belt and sprocket sold under the name of Flex-e-Gear by the Winfred M. Berg company. This type of mechanical linkage possesses zero backlash and is vibrationally much quieter than gears.

The rotational degree of freedom is linked to the motor by a friction drive system. It would be advantageous to replace this system with the same type belt and sprocket arrangement as mentioned above. This would eliminate the inherent unreliability of the present system.

5.2 Electronic Improvements to the Control System

The control system electronics are for the most part an optimal solution to the control problem. The weakest link in the hardware is the Motor Power Driver Card. This card is troublesome in that the power transistors do not turn off as

fast as they should. When switching times are slow, the power dissipation rises due to a momentary short across the power supply, through the transistors. It is suggested that some high-power switching transistors are obtained to replace the main power transistors. Another solution could be the replacement of these bipolar transistors with power FET's.

The power supply used in the system provides +5 volts at up to 6 amps of current. At the start of this project it was difficult to predict the final power consumption of the complete system. It is now apparent that the 6 amp supply is being strained by the requirements of the system. A Power-One 5 volt 12 amp supply would take care of the system power requirements and provide additional headroom for system additions.

The system components are contained in two chassis that provide no ventilation. It is strongly suggested that fans be mounted on both the power driver chassis and the control system chassis to provide adequate ventilation.

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